

FIG. 1A
(Prior Art)

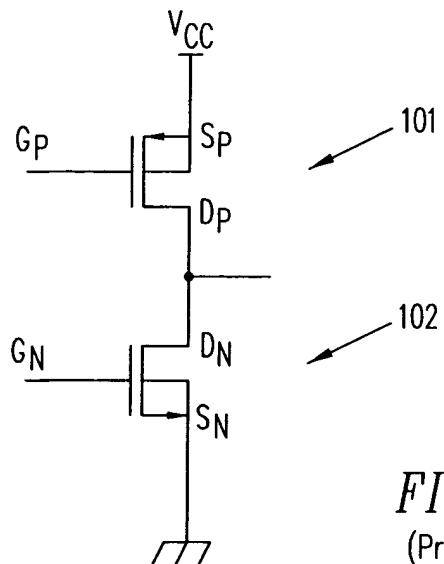


FIG. 1B
(Prior Art)

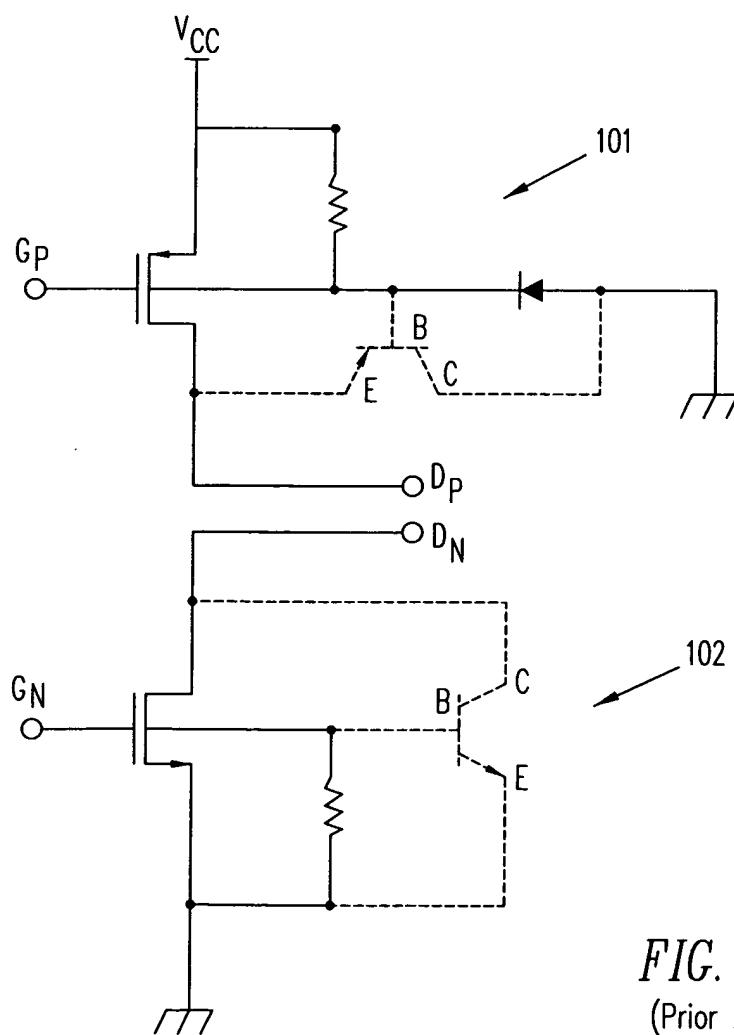
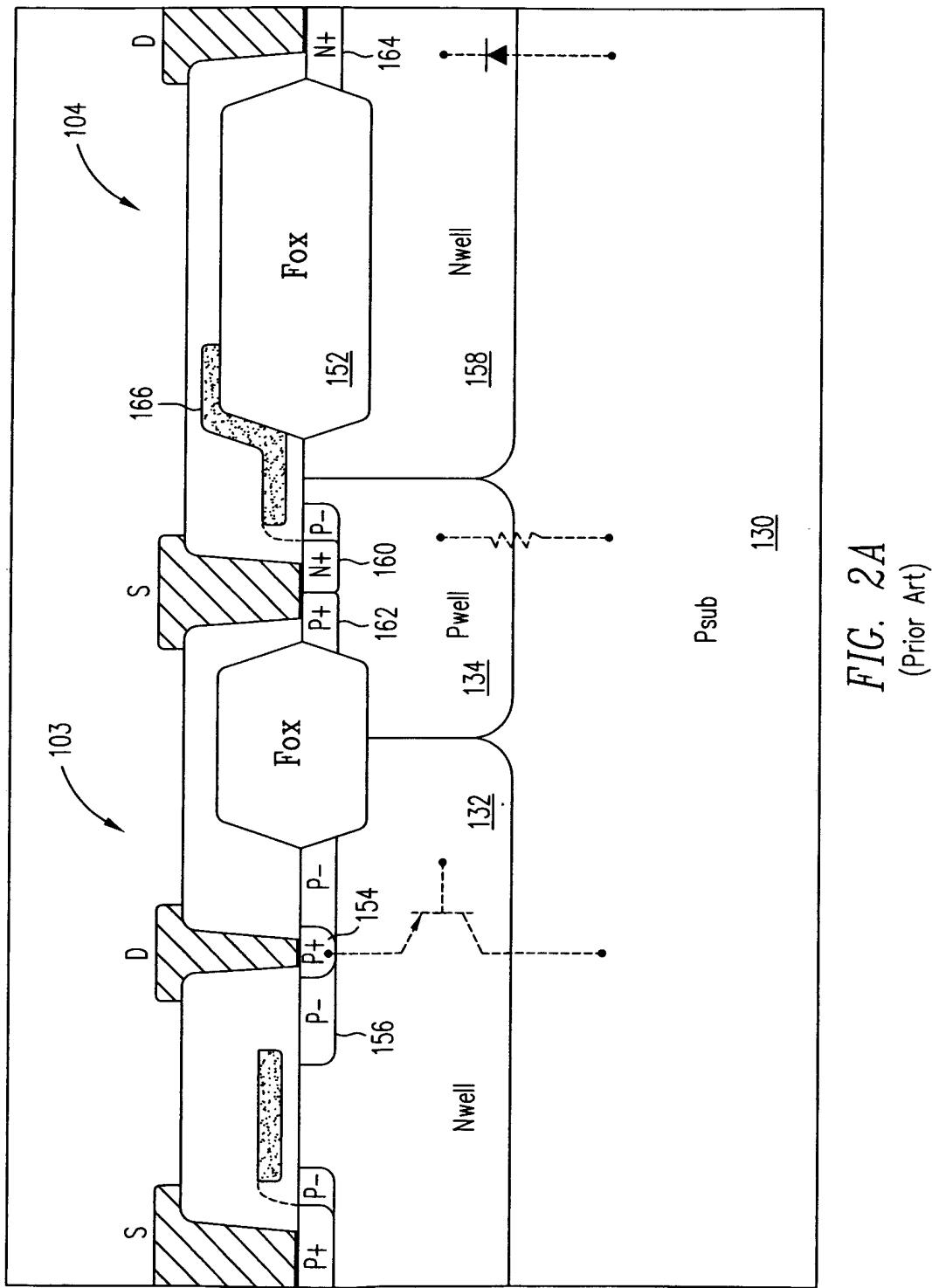
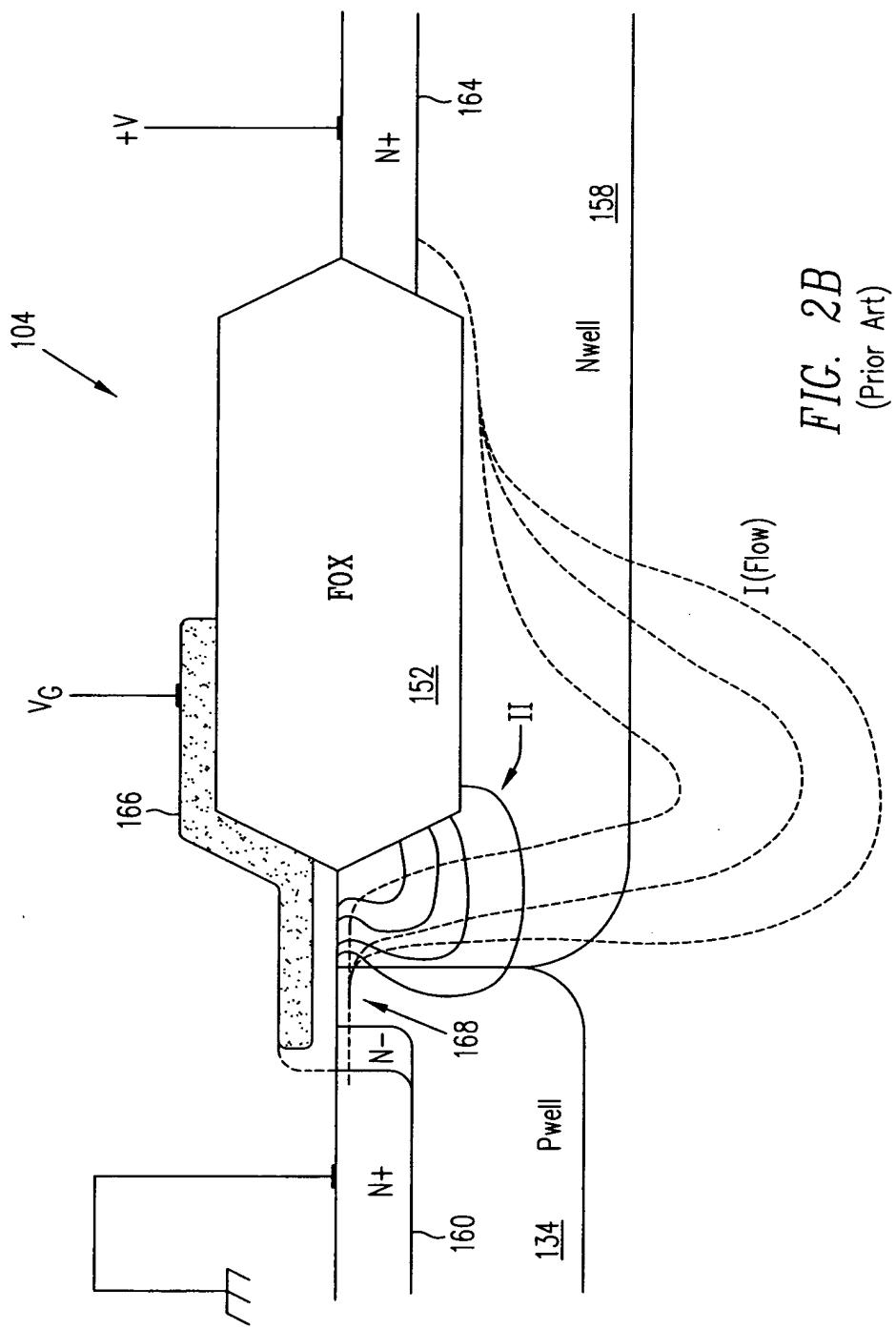


FIG. 1C
(Prior Art)





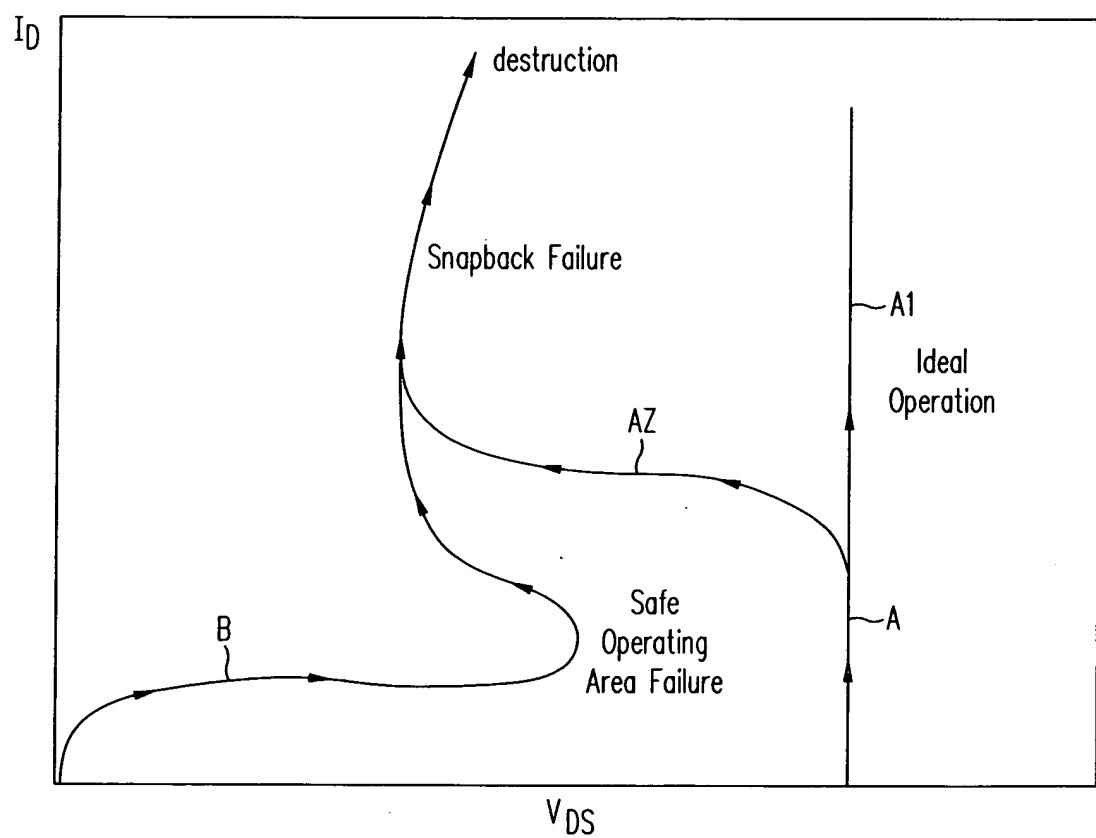


FIG. 2C
(Prior Art)

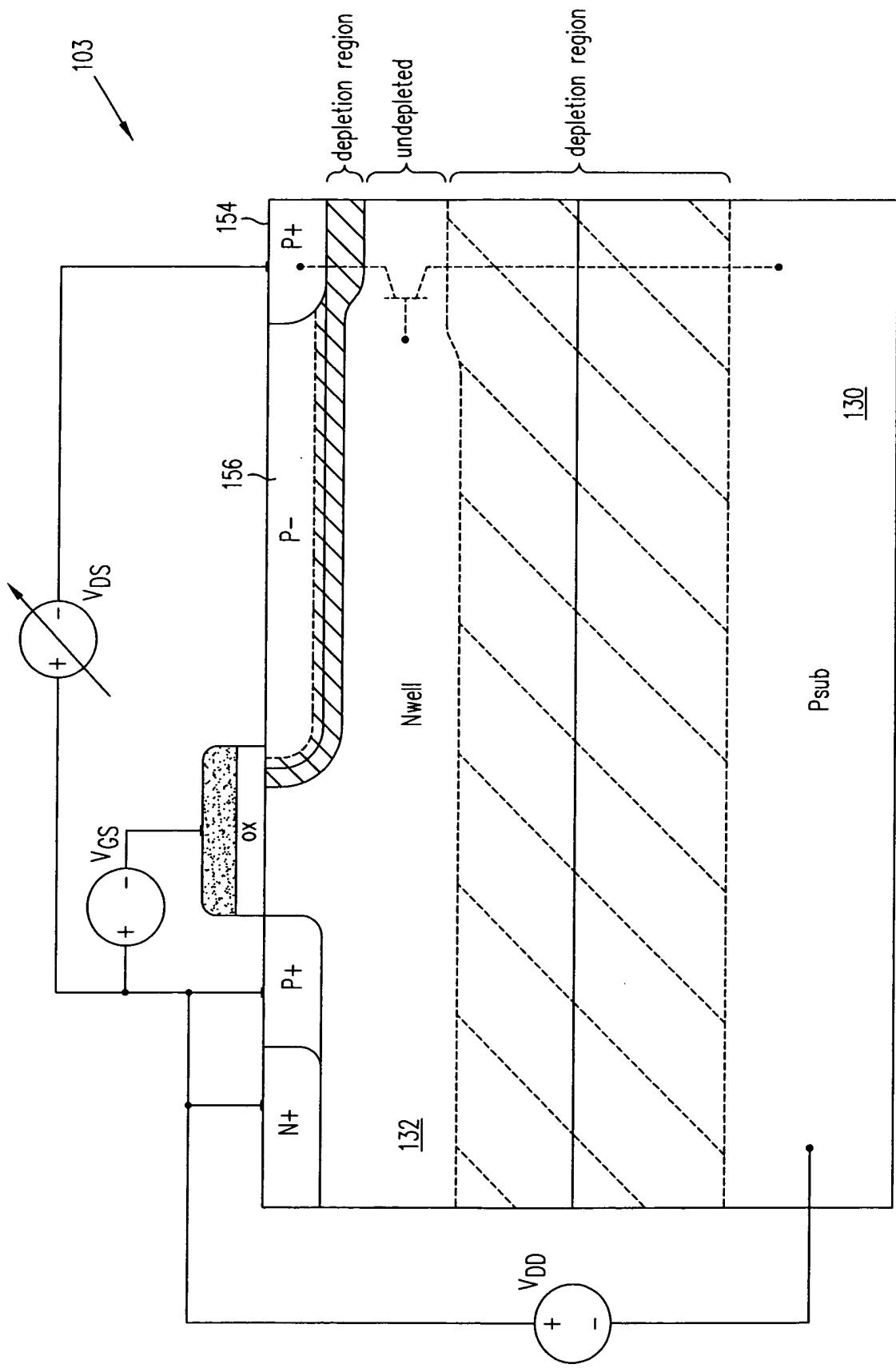


FIG. 2D (Prior Art)

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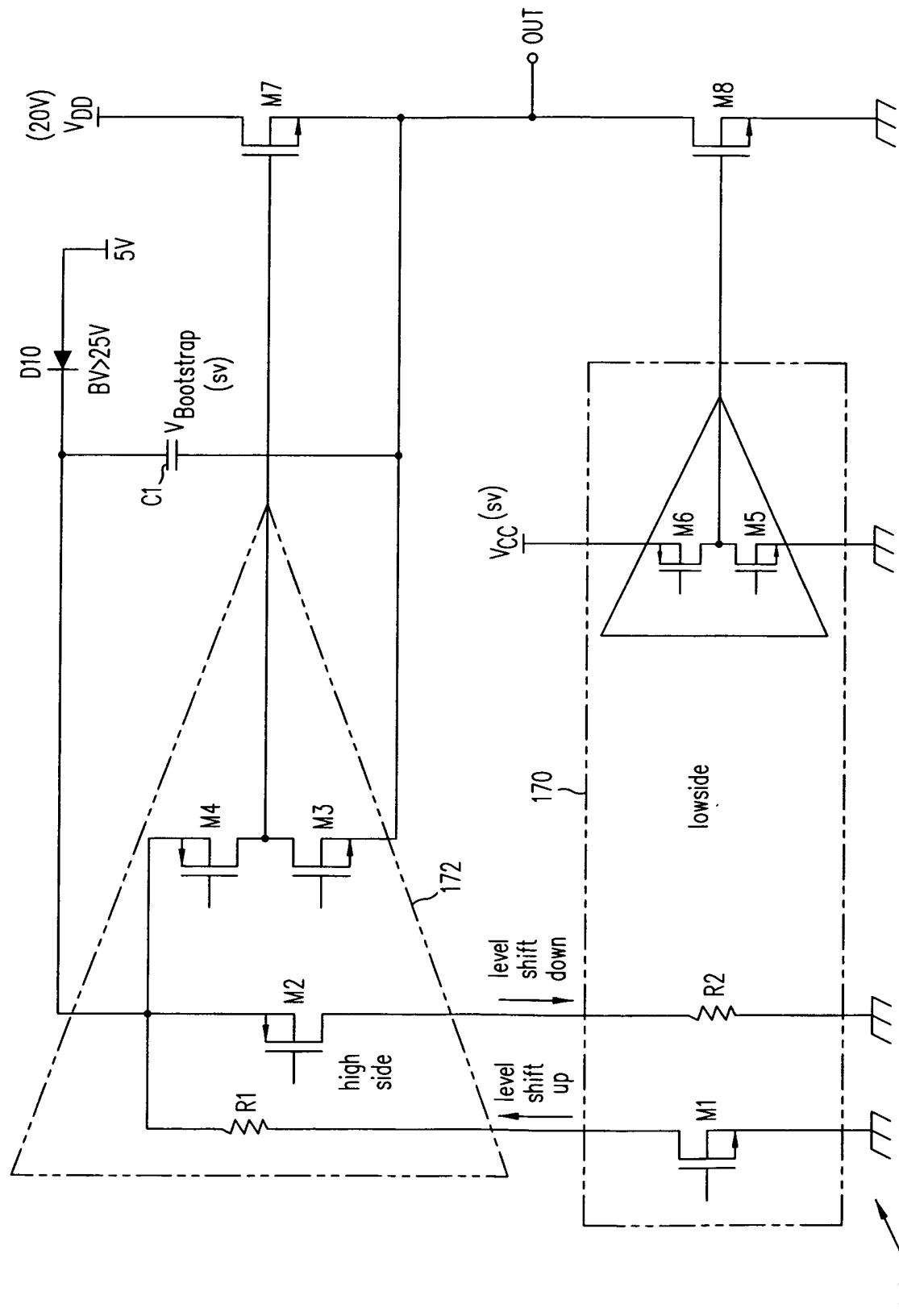


FIG. 3 (Prior Art)
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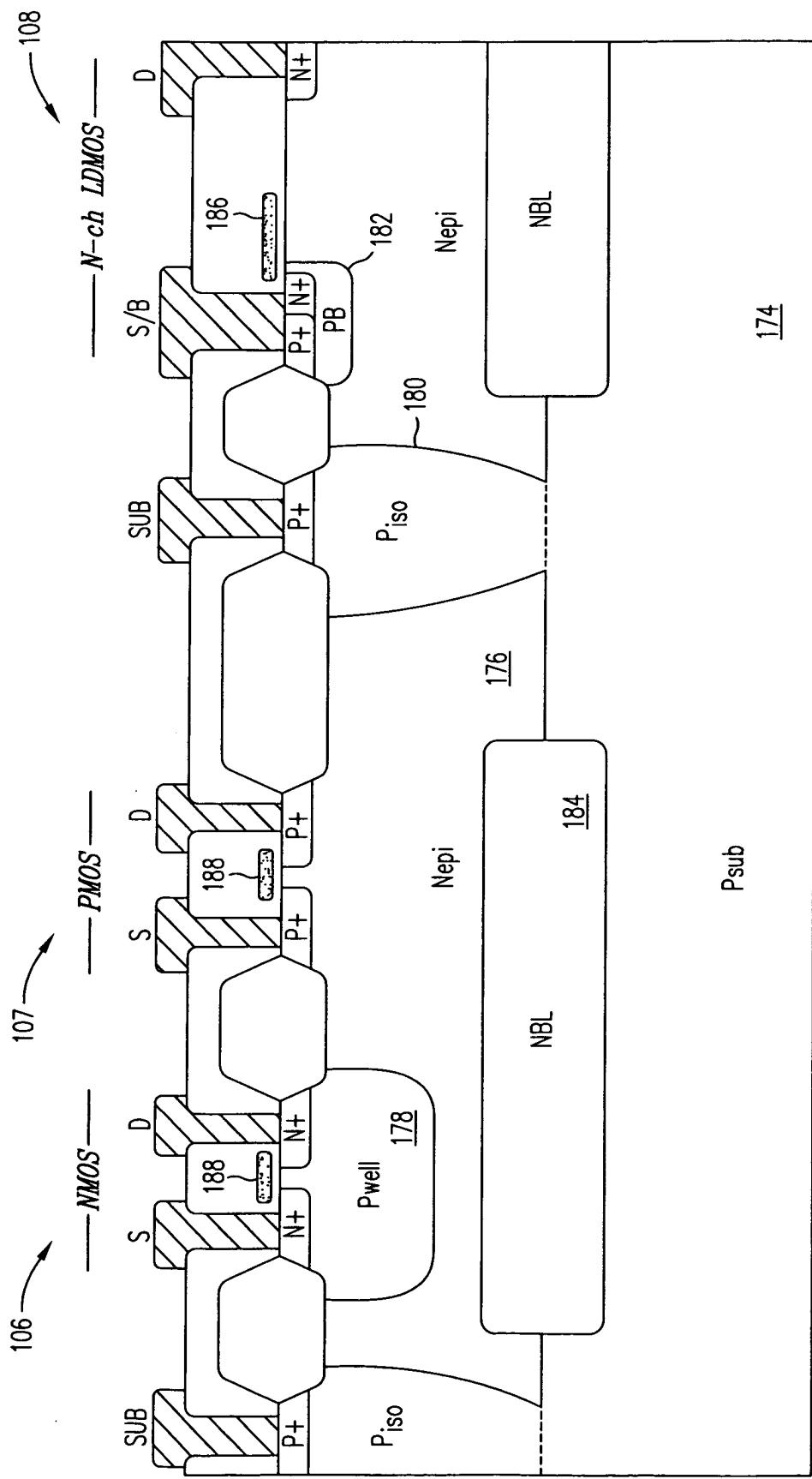


FIG. 4A
(Prior Art)

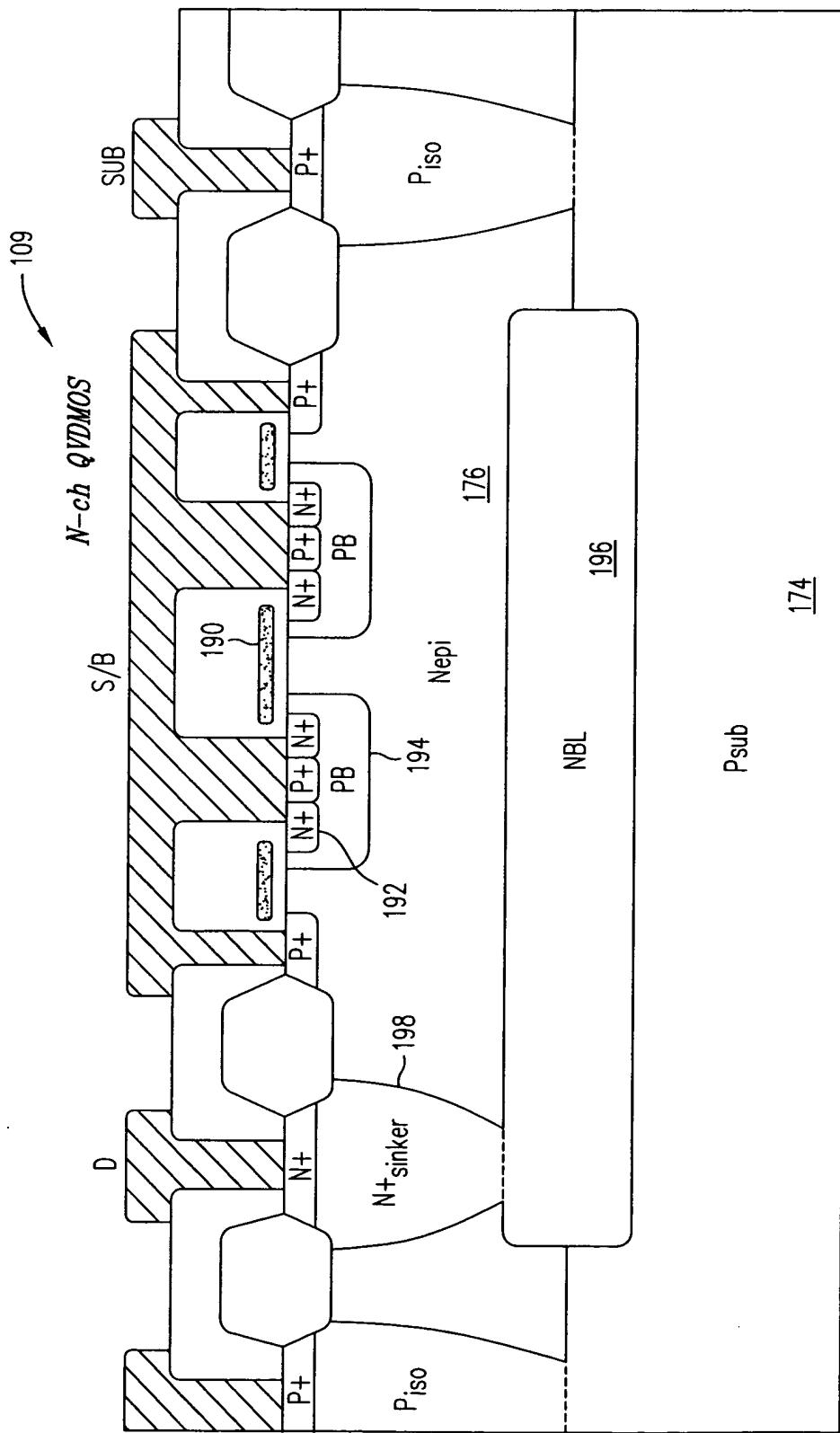


FIG. 4B
(Prior Art)

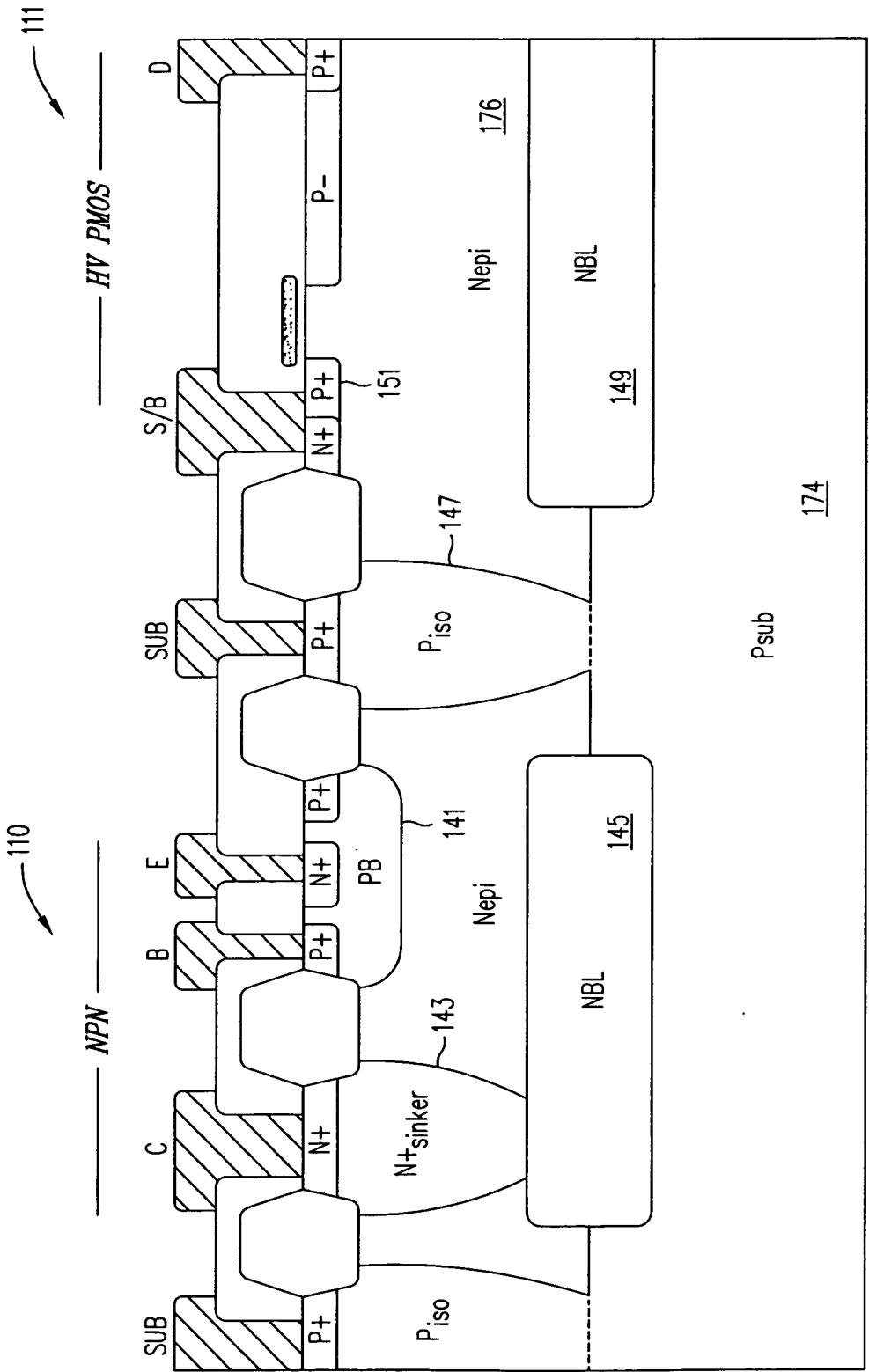


FIG. 4C
(Prior Art)

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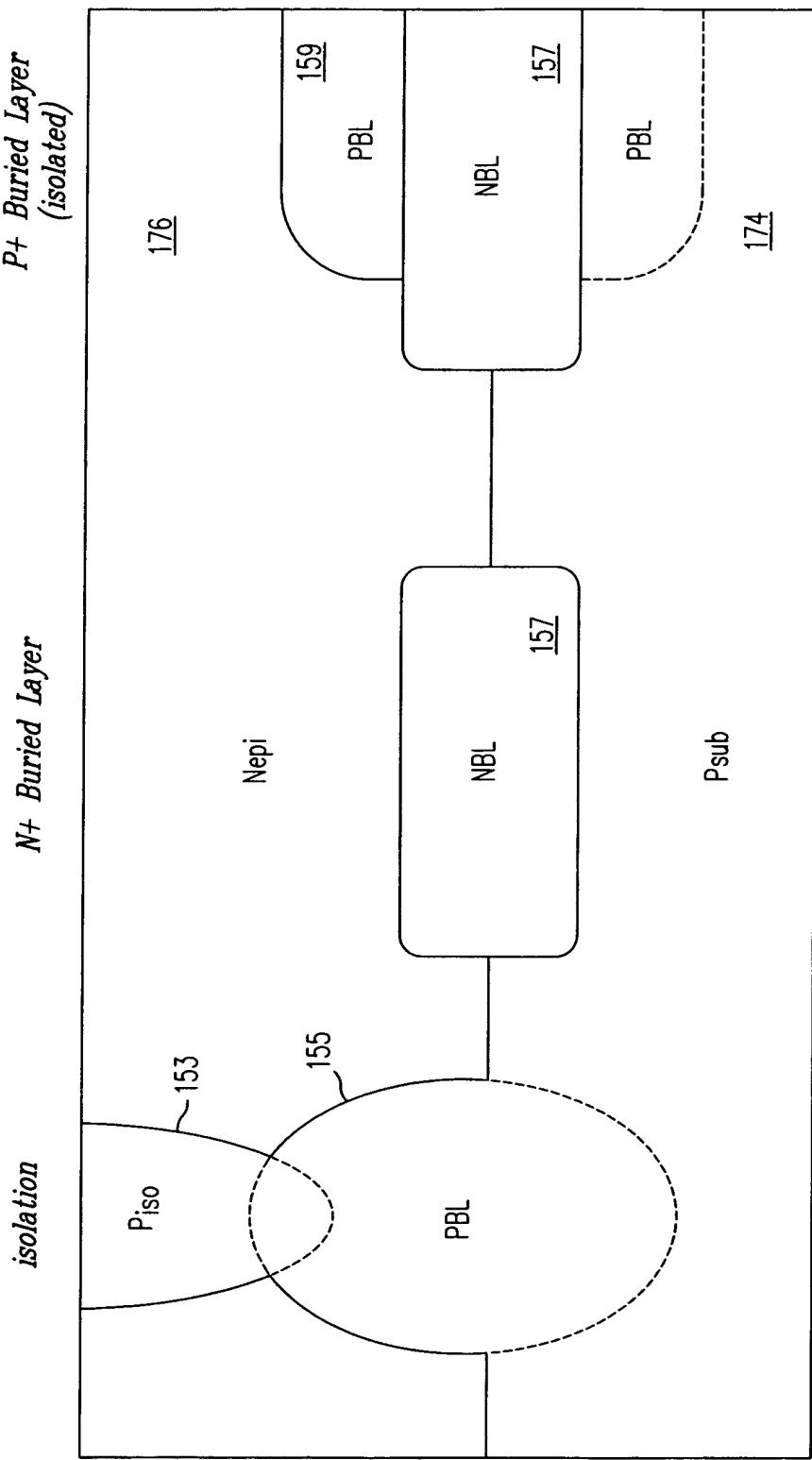


FIG. 5A
(Prior Art)

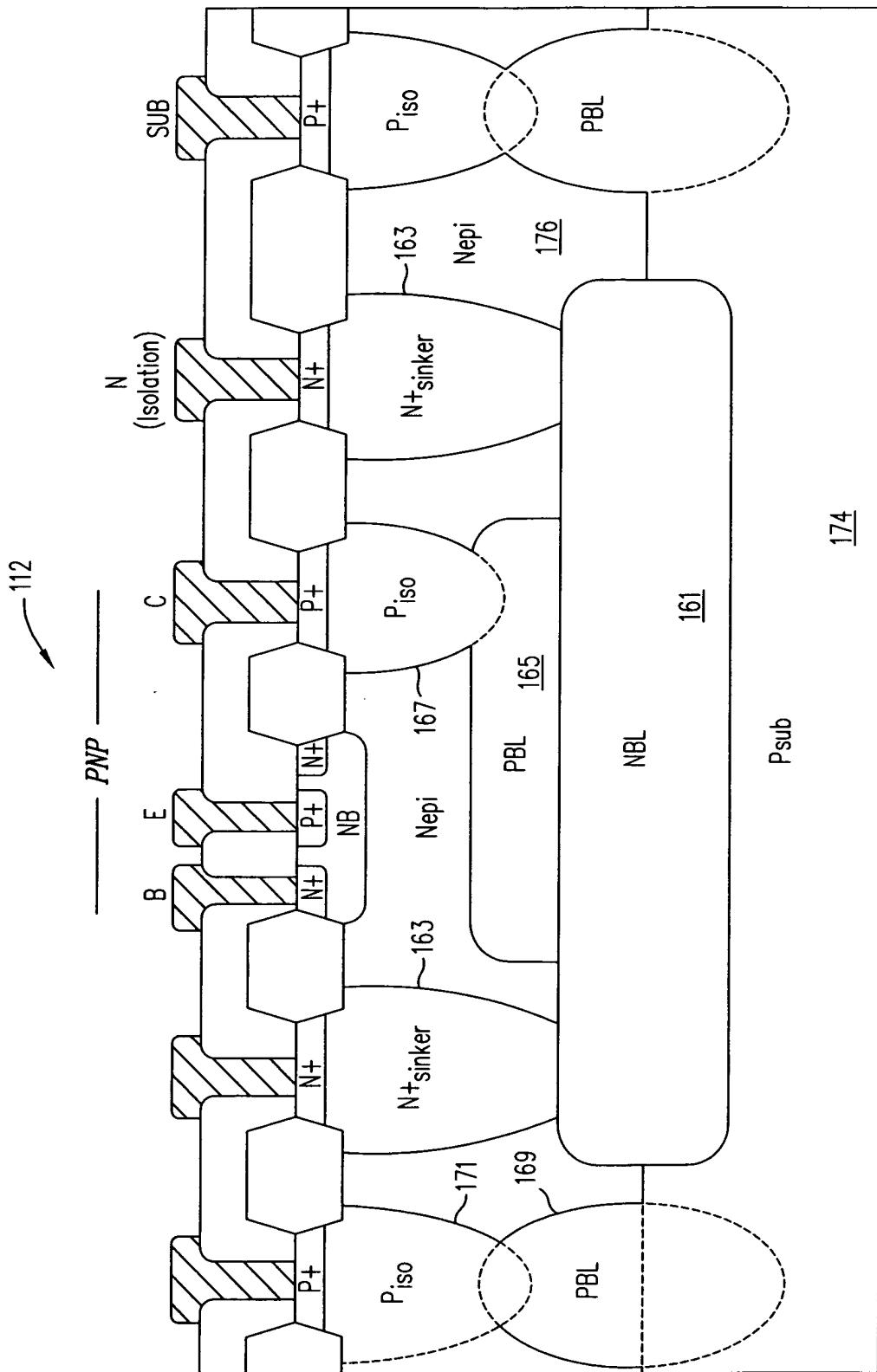
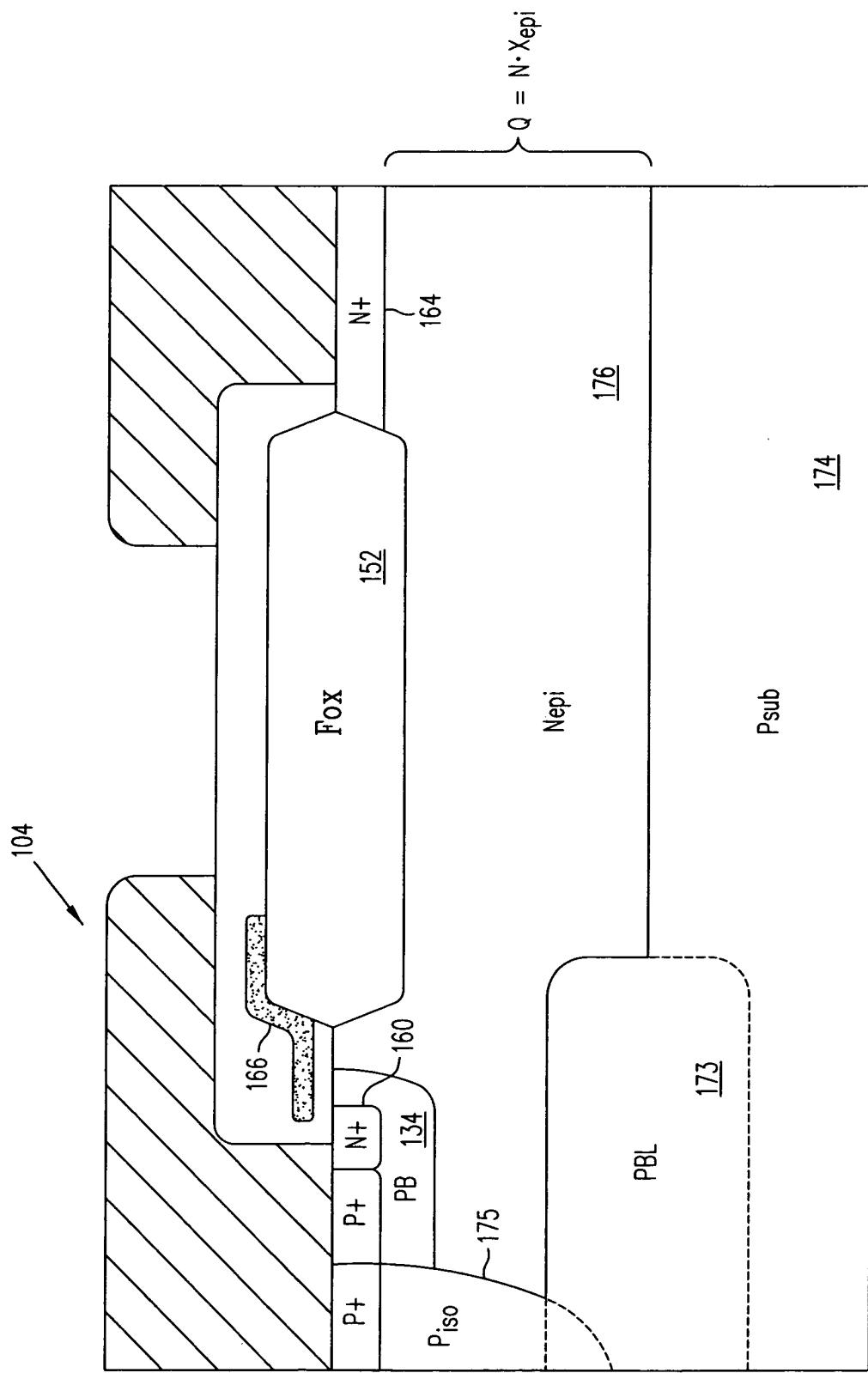


FIG. 5B
(Prior Art)



*FIG. 5C
(Prior Art)*

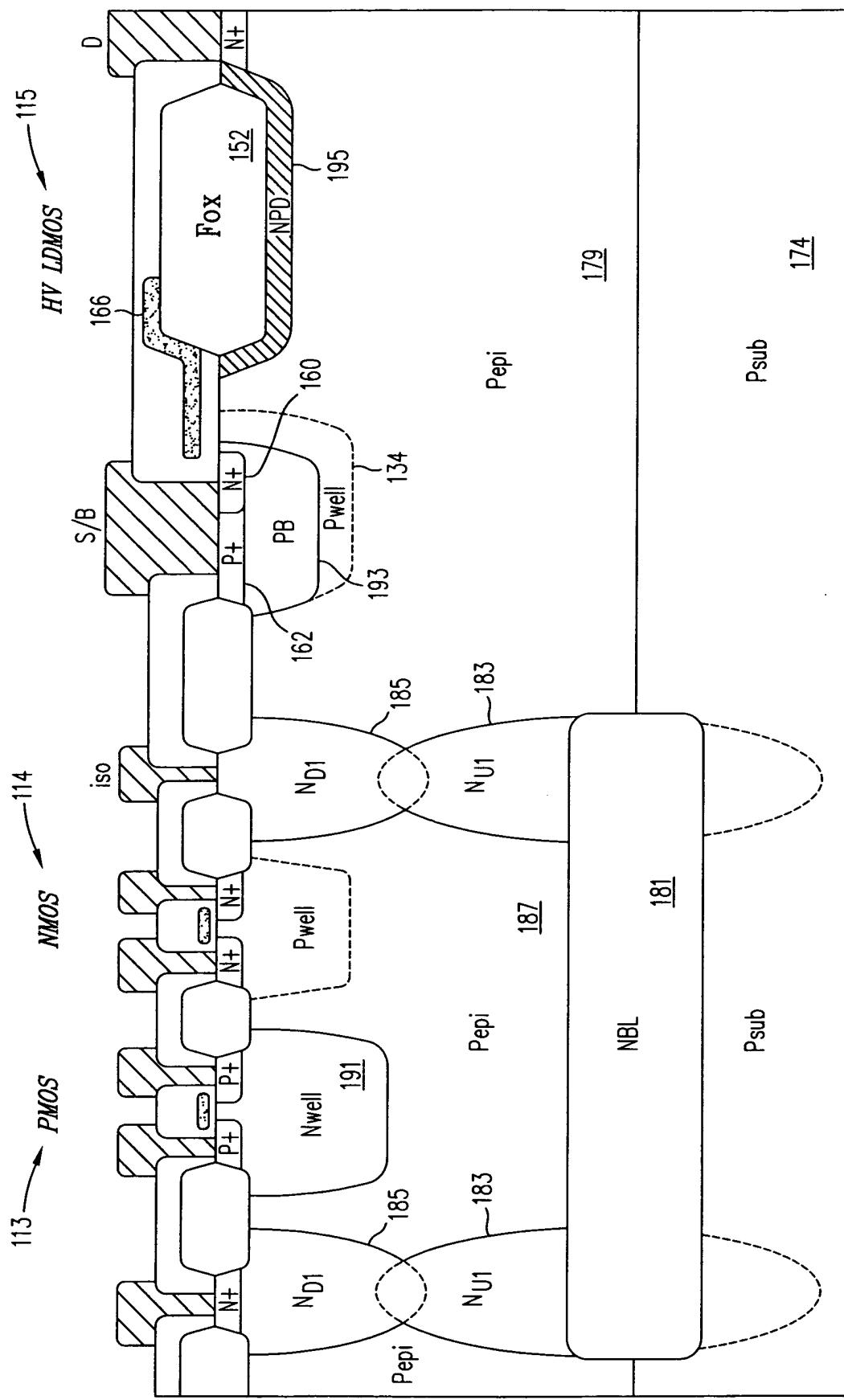


FIG. 6A (Prior Art)

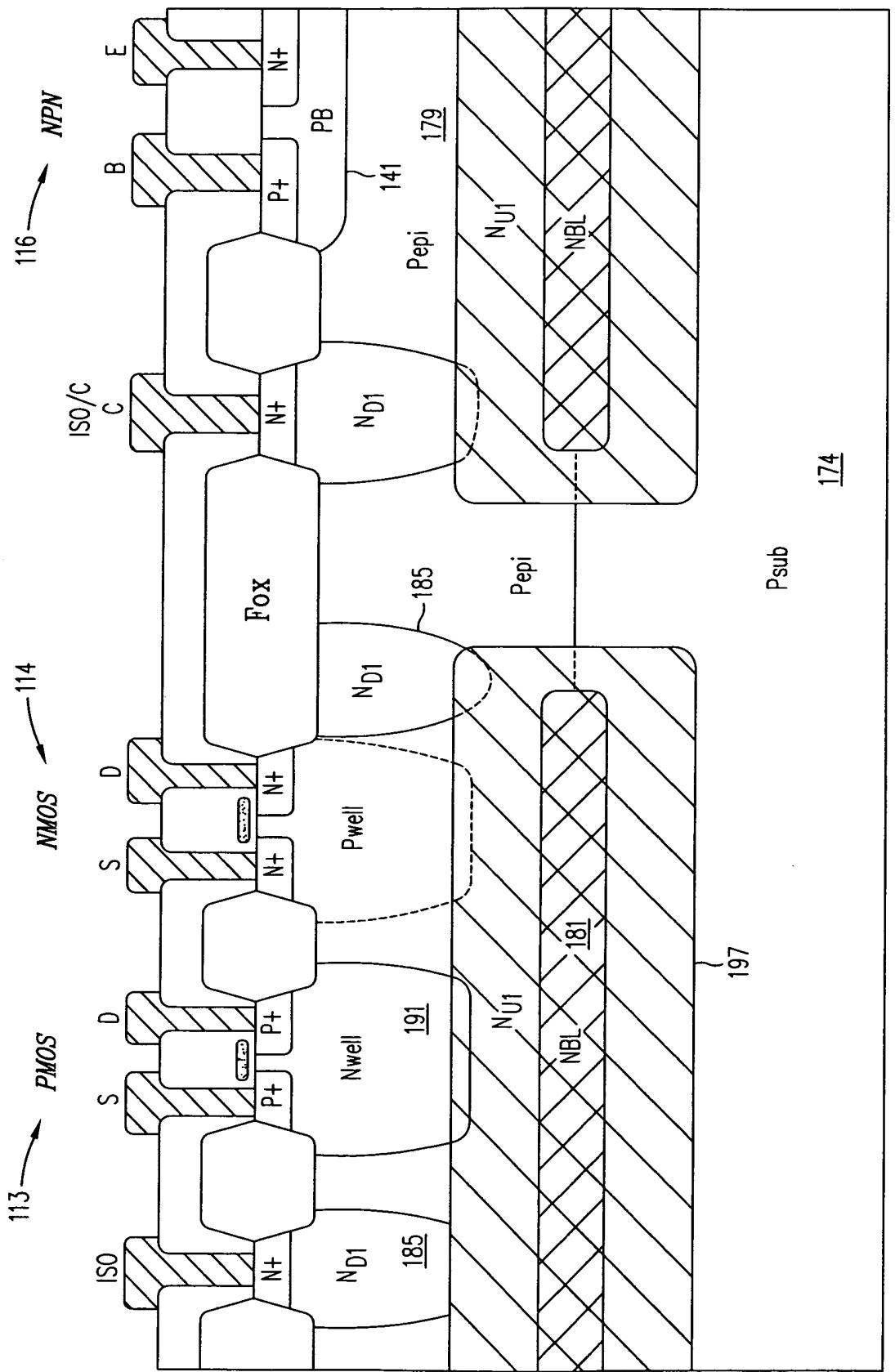


FIG. 6B (Prior Art)

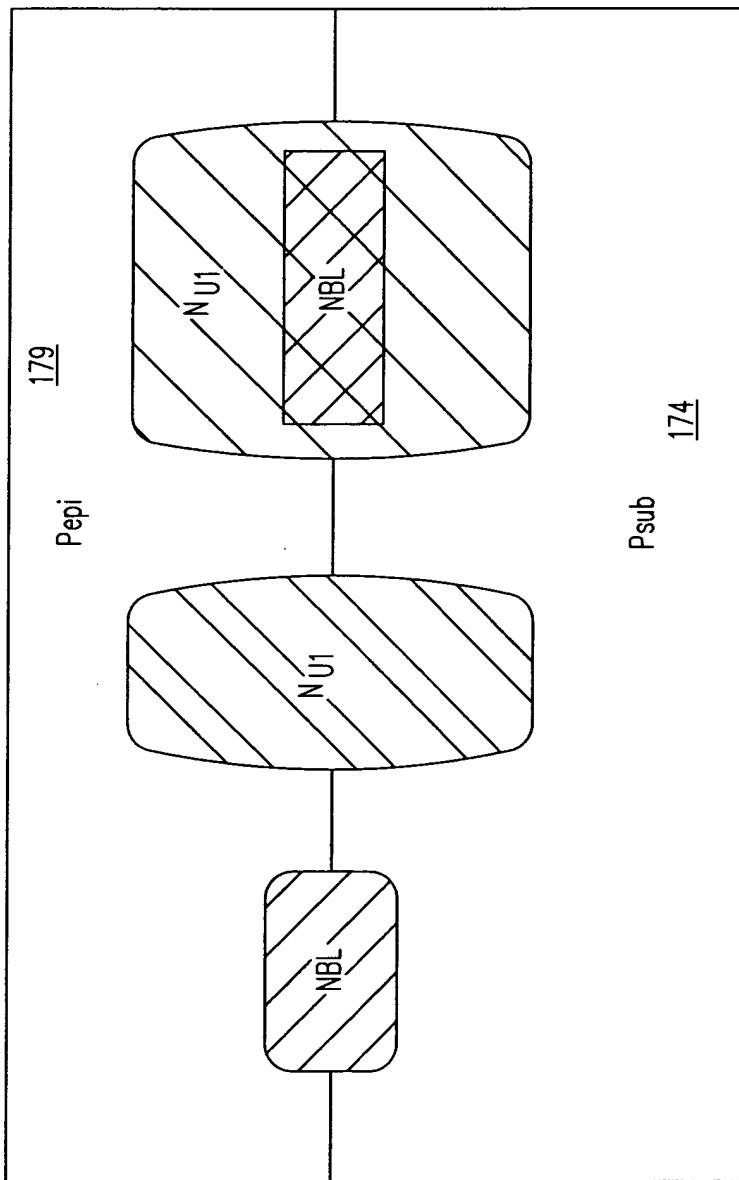


FIG. 6C
(Prior Art)

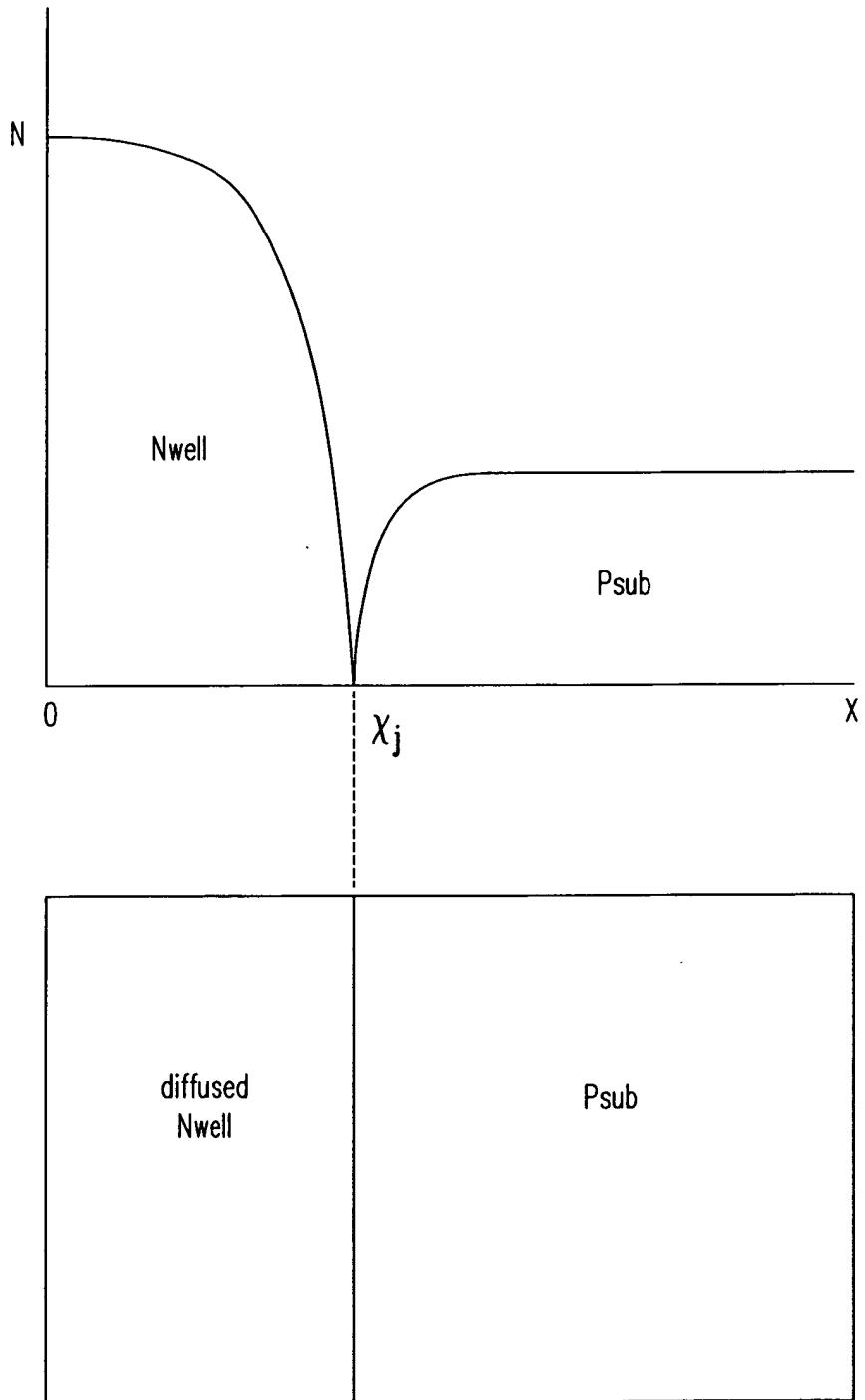


FIG. 7A
(Prior Art)

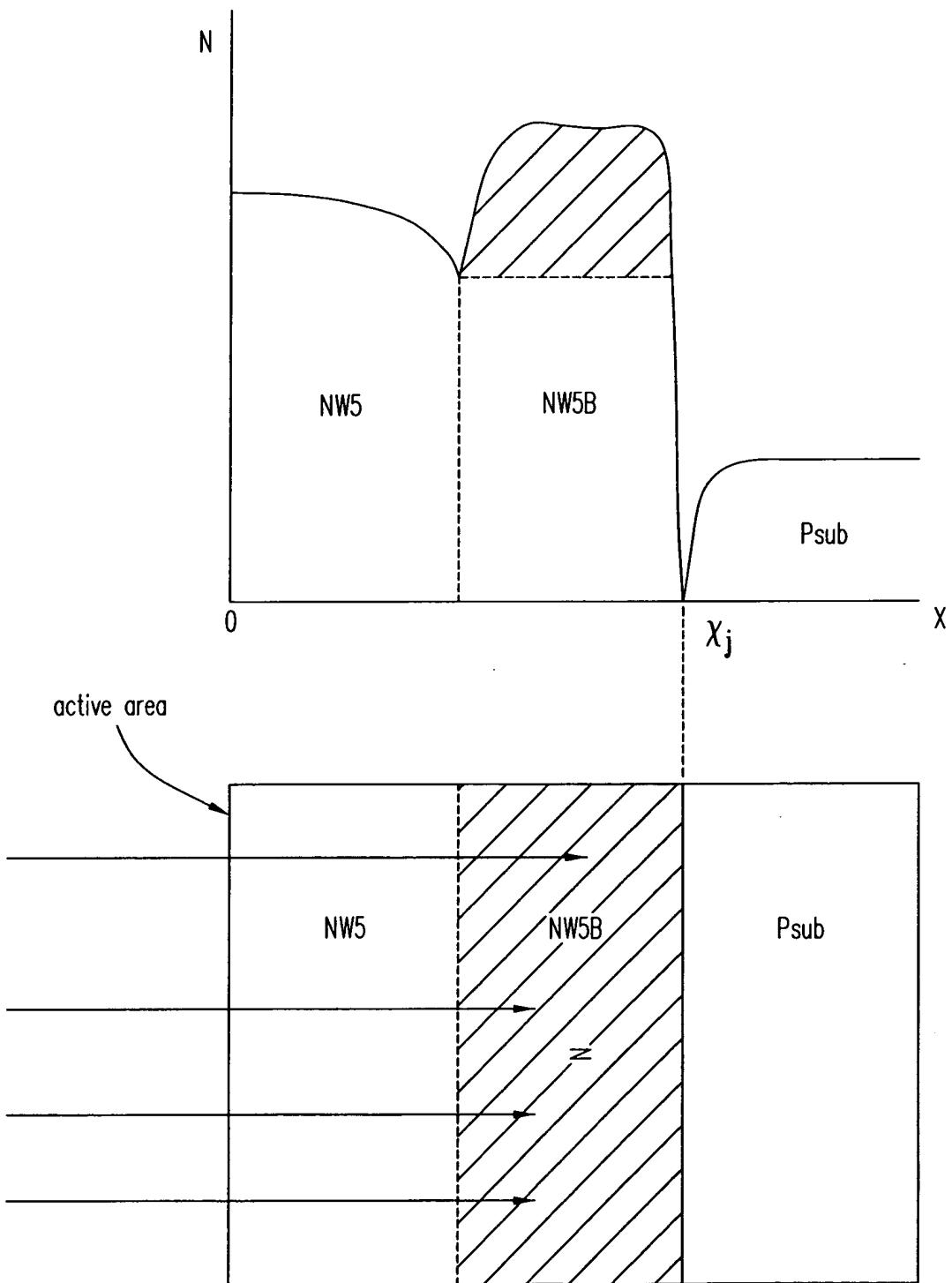


FIG. 7B

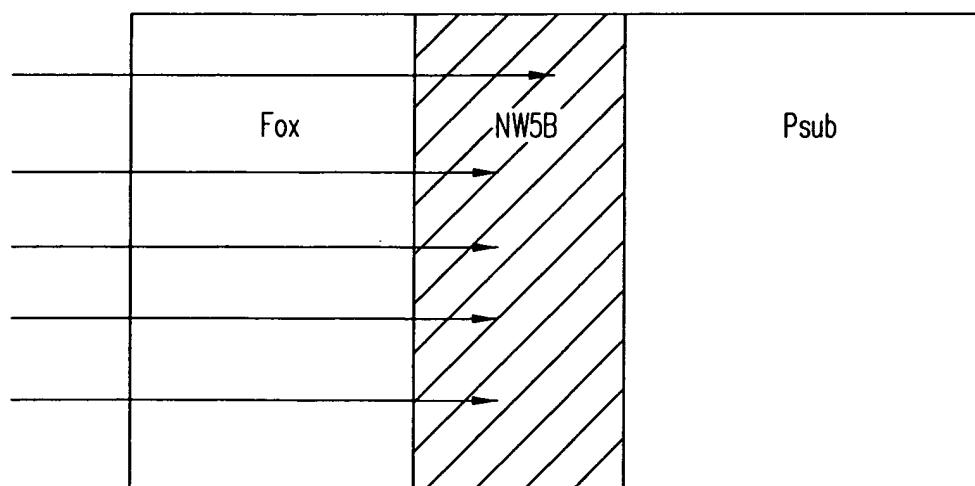
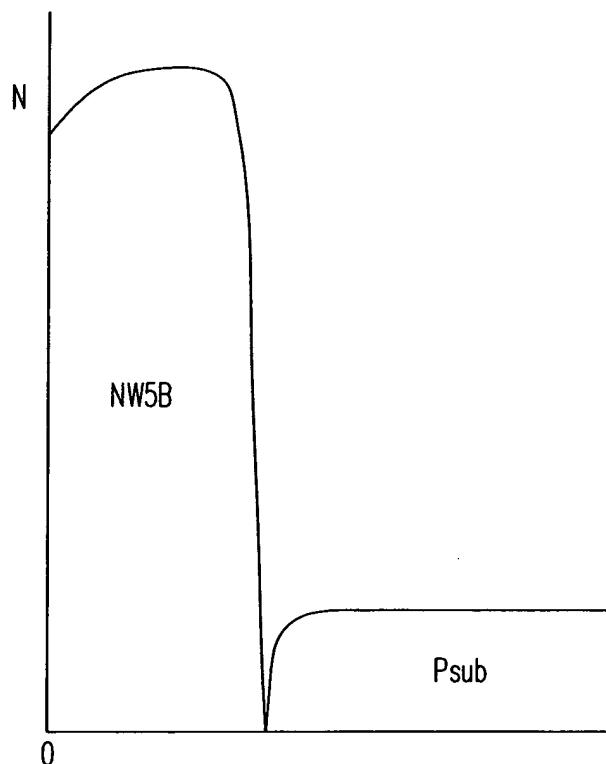


FIG. 7C

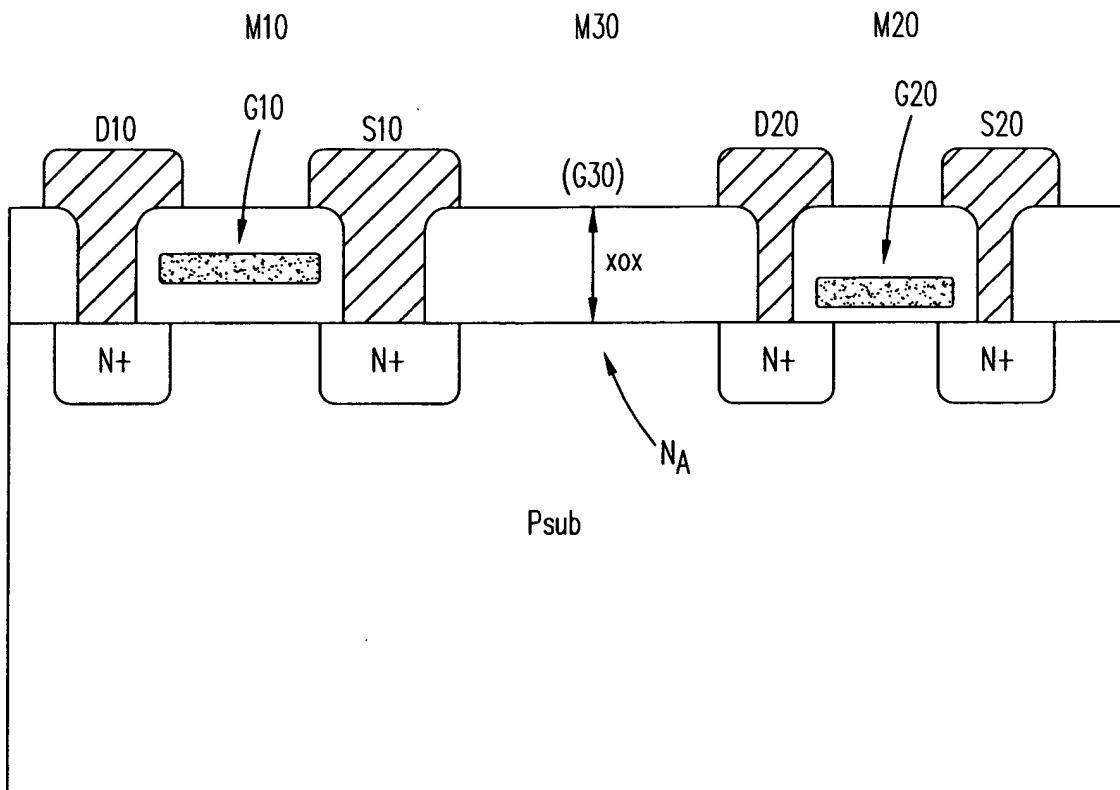


FIG. 8A

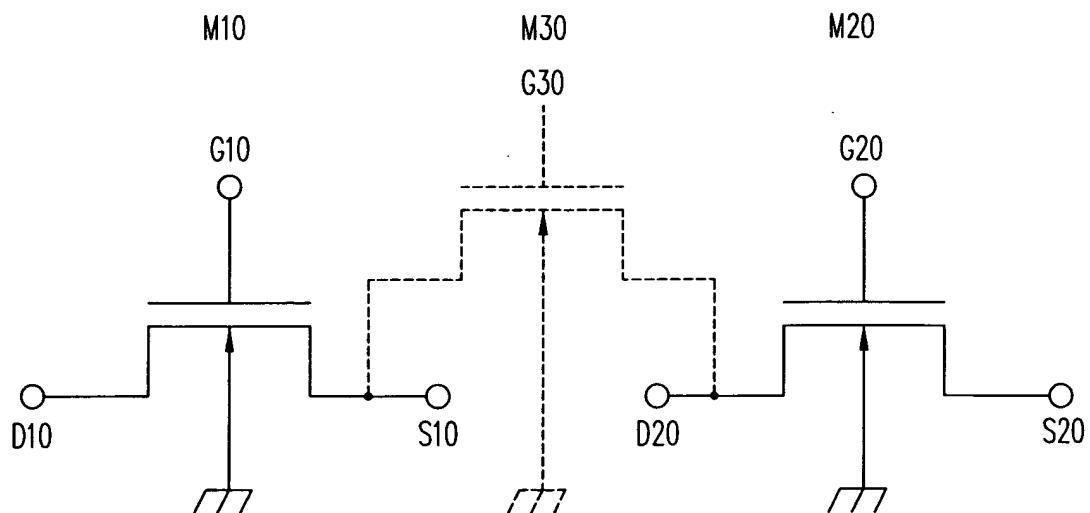


FIG. 8B

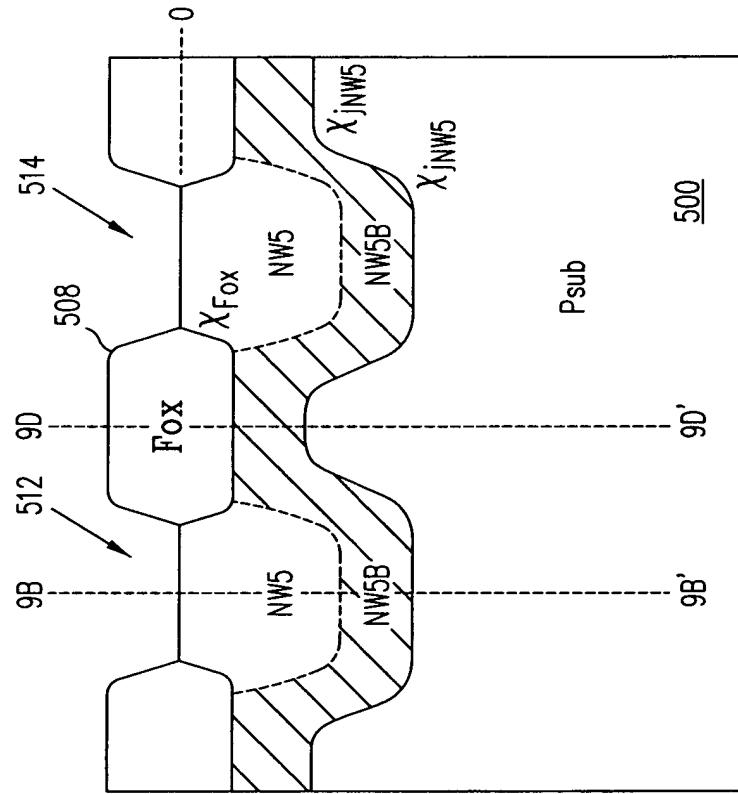
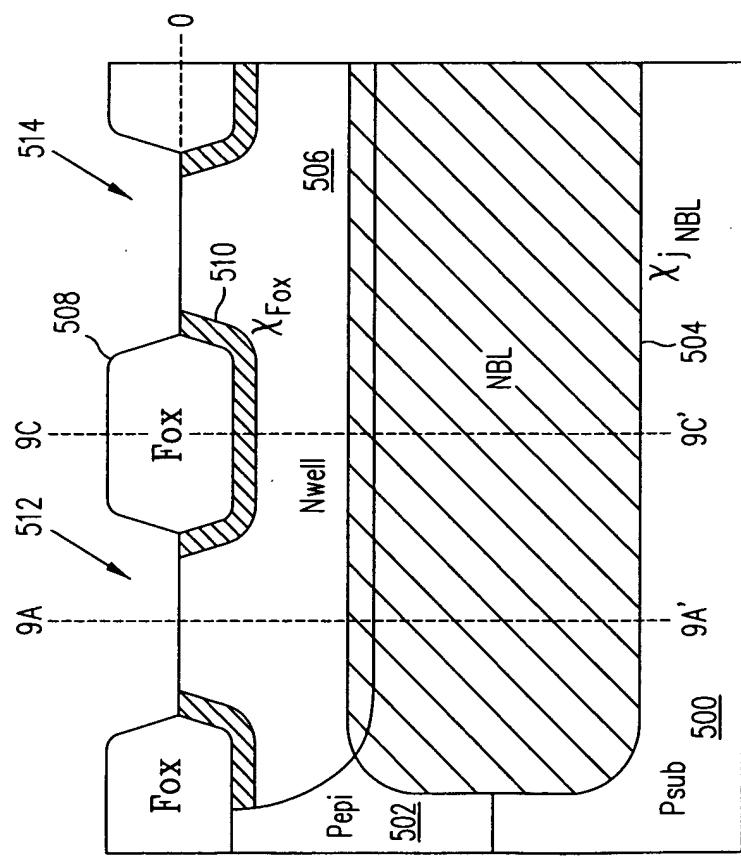


FIG. 9B

FIG. 9A
(Prior Art)

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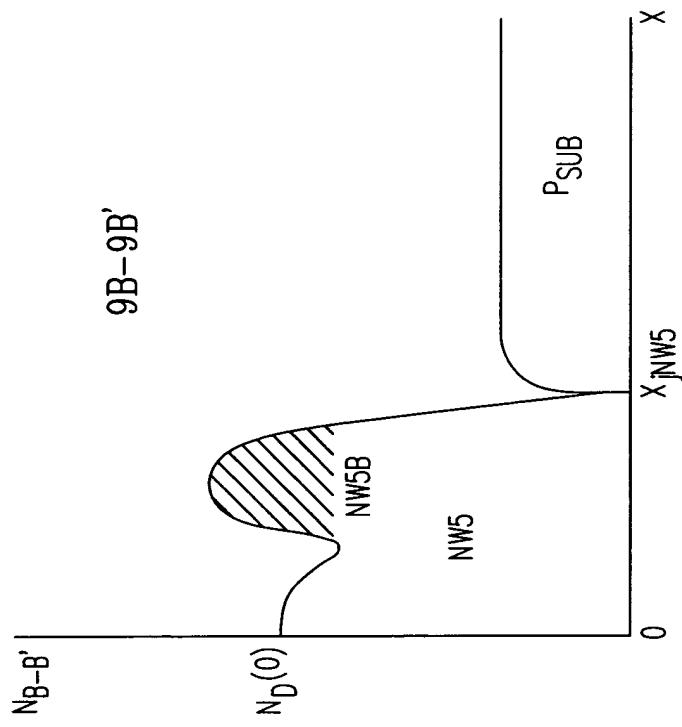


FIG. 9D

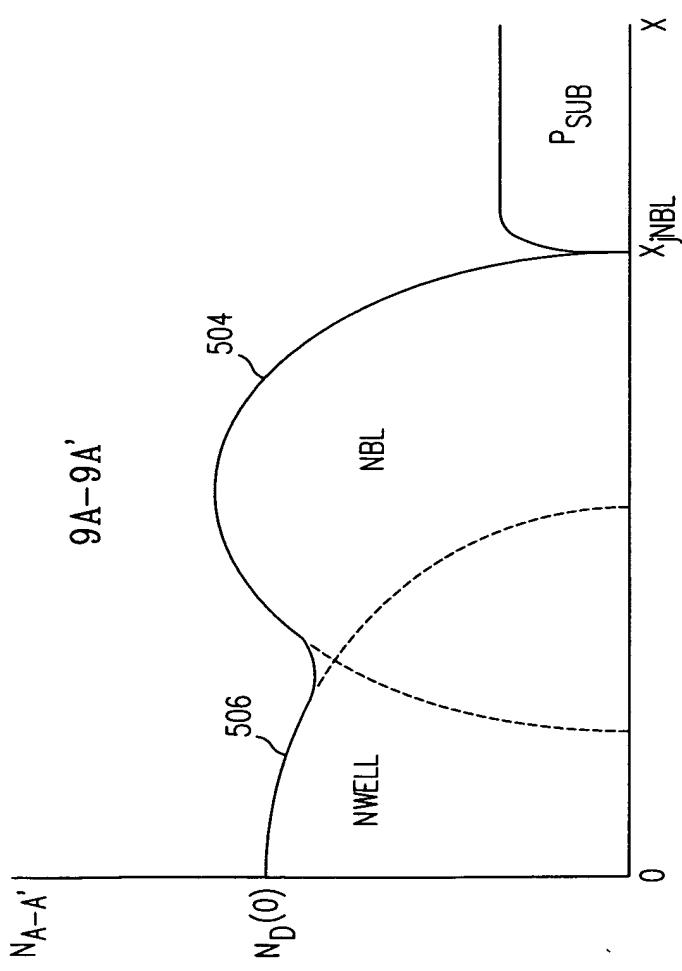


FIG. 9C
(Prior Art)

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FIG. 9E
(Prior Art)

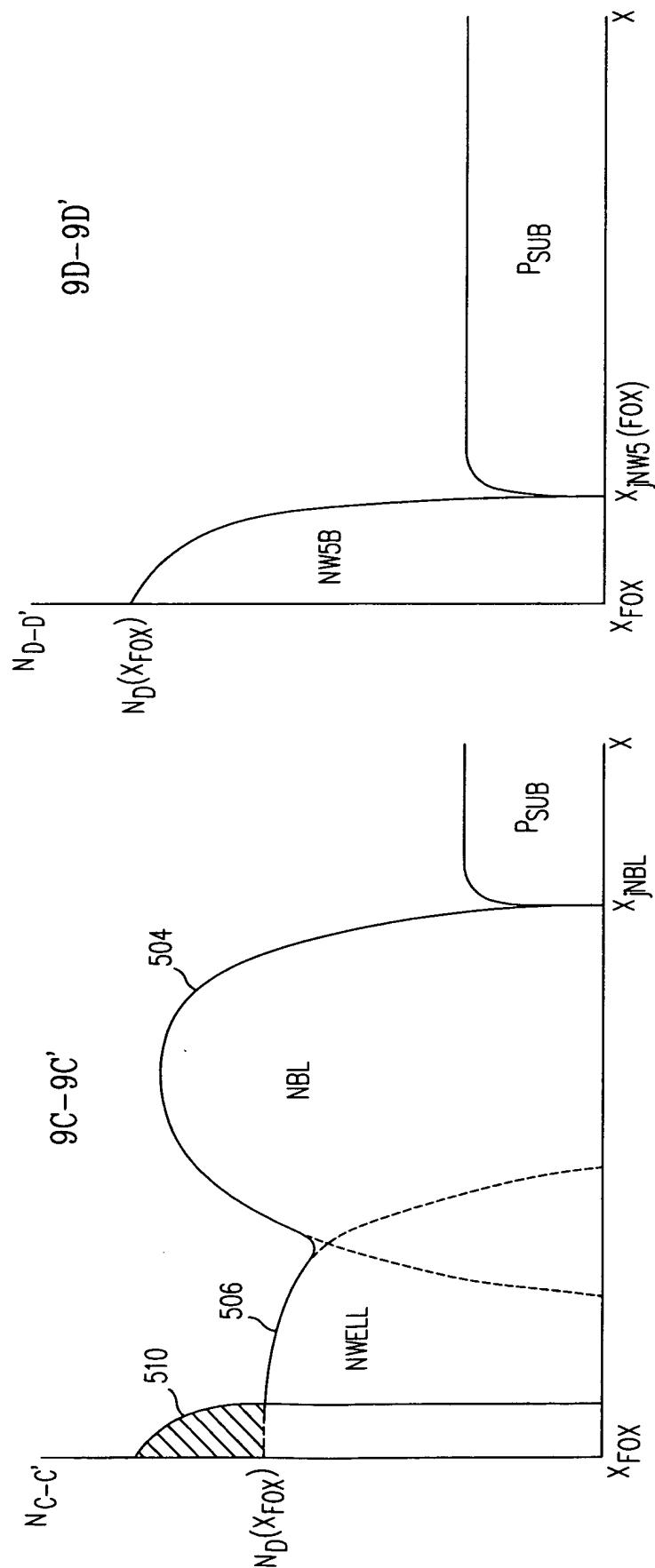


FIG. 9F

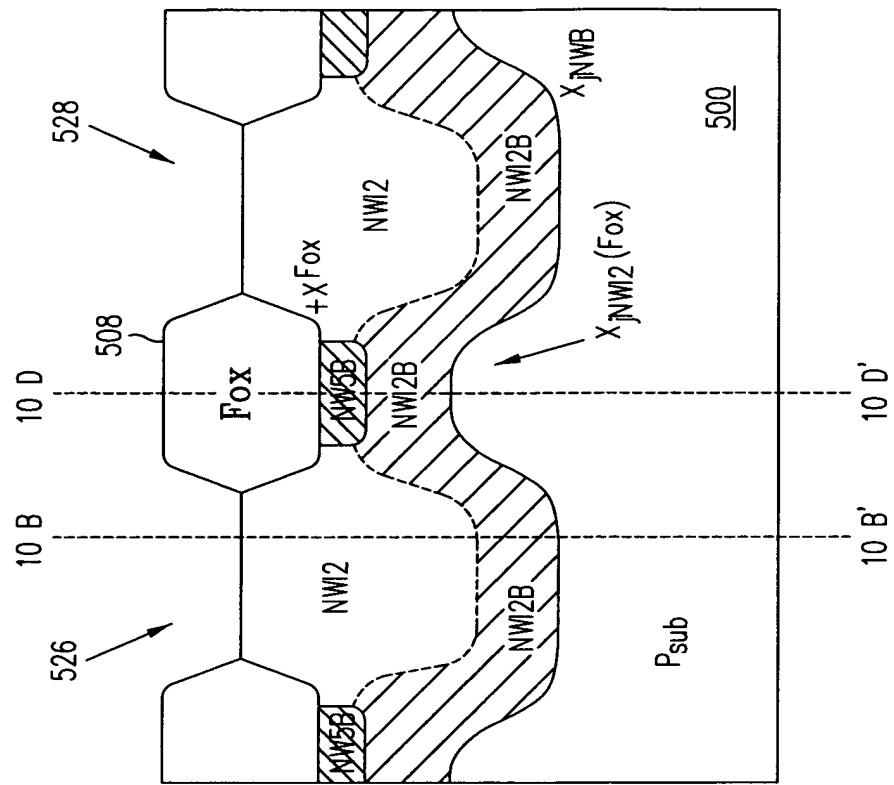


FIG. 10B

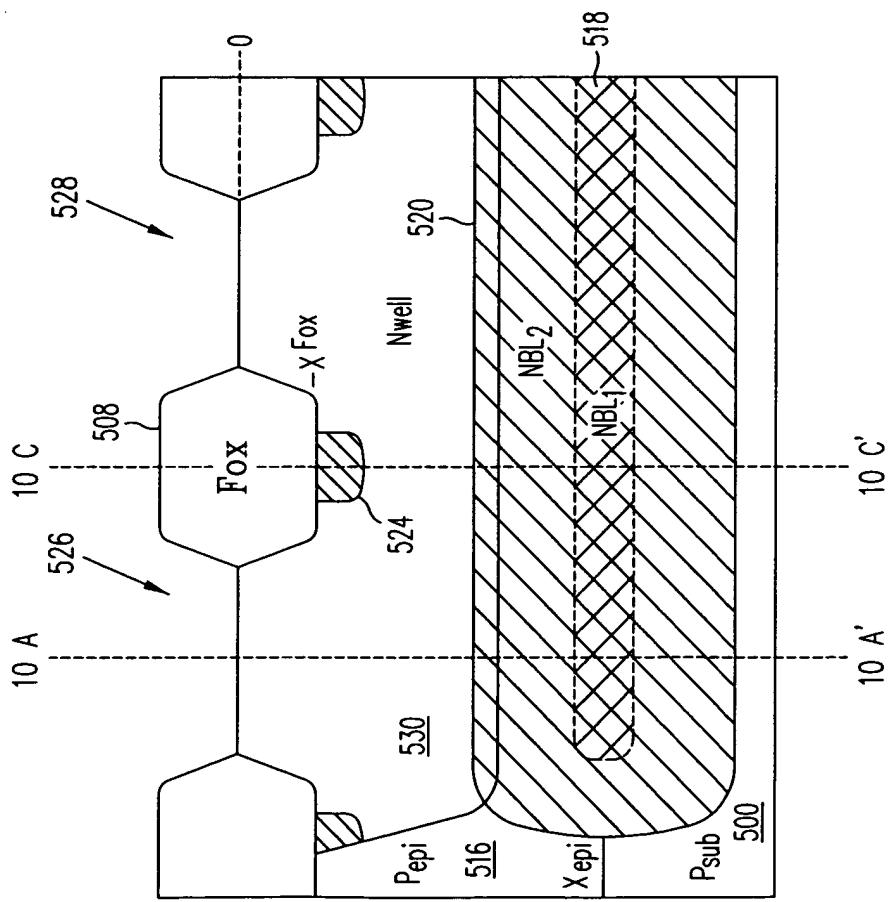
FIG. 10A
(Prior Art)



FIG. 10C
(Prior Art)

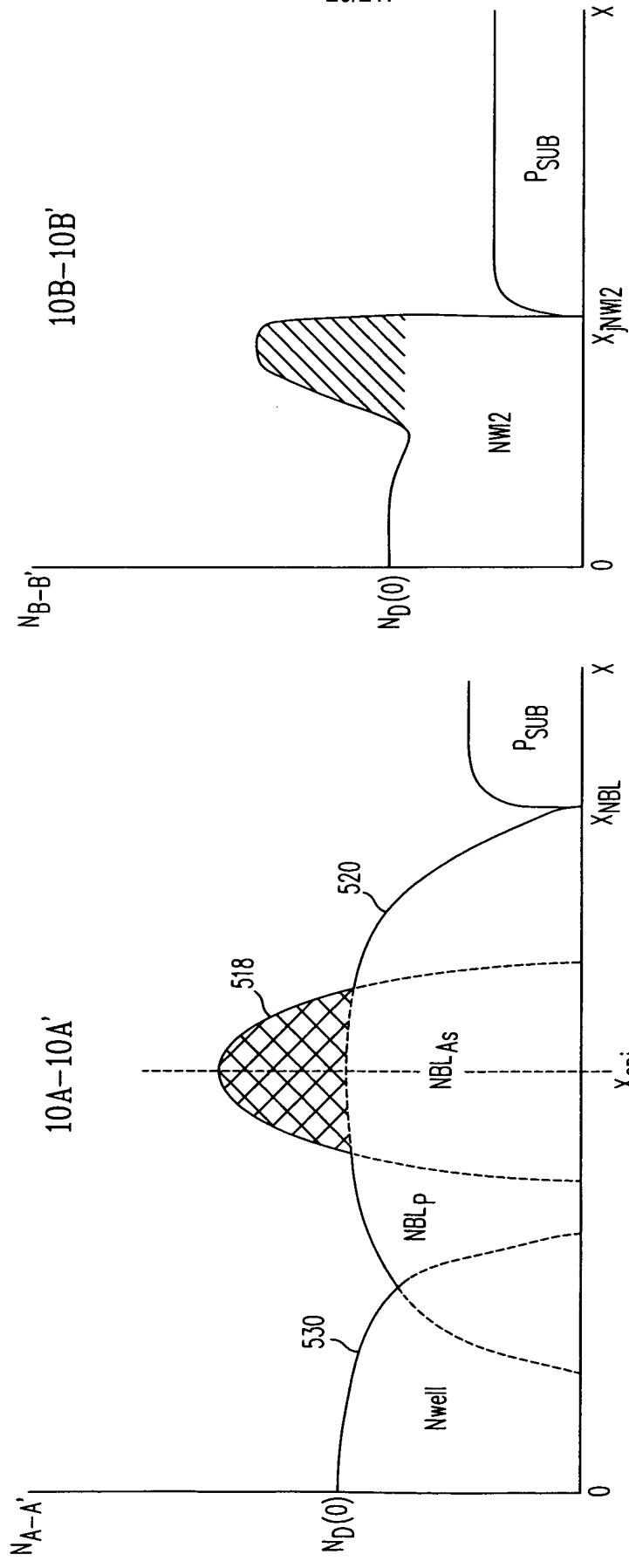


FIG. 10D

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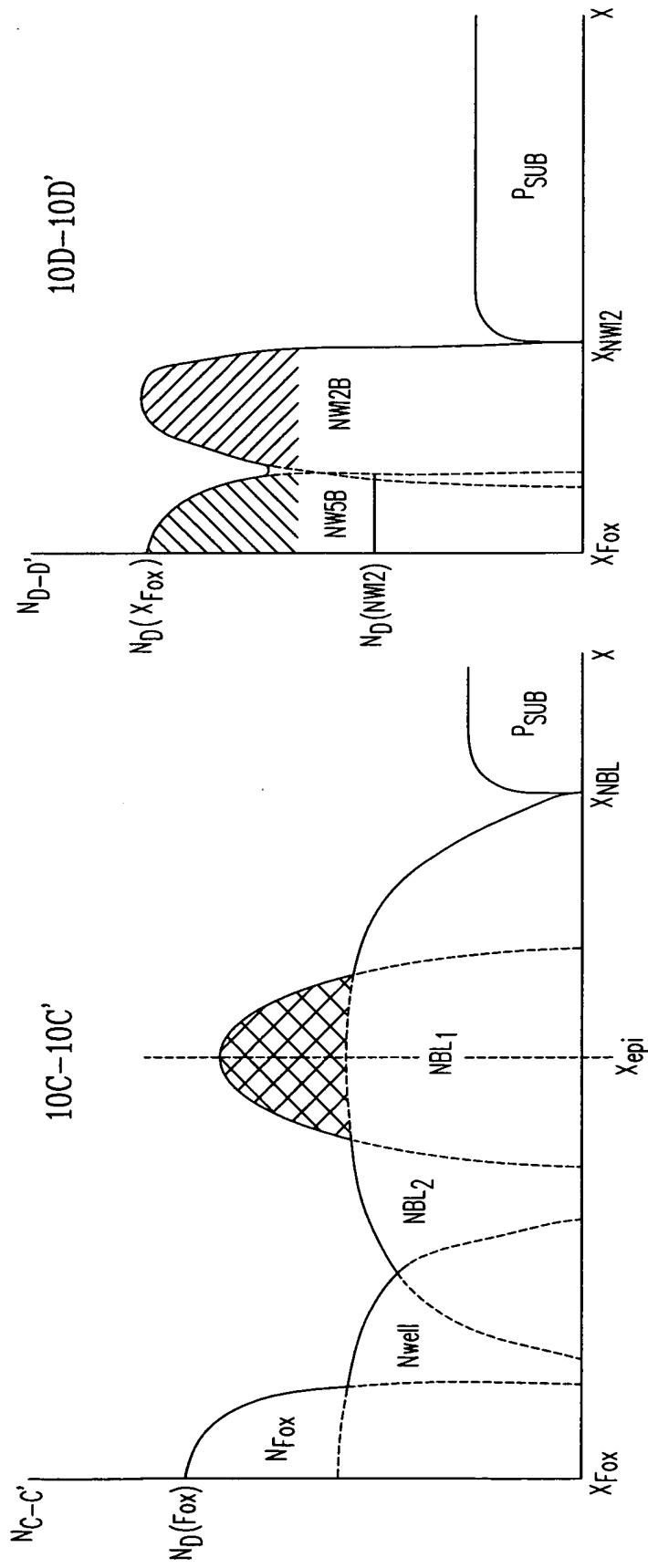


FIG. 10E
(Prior Art)

FIG. 10F

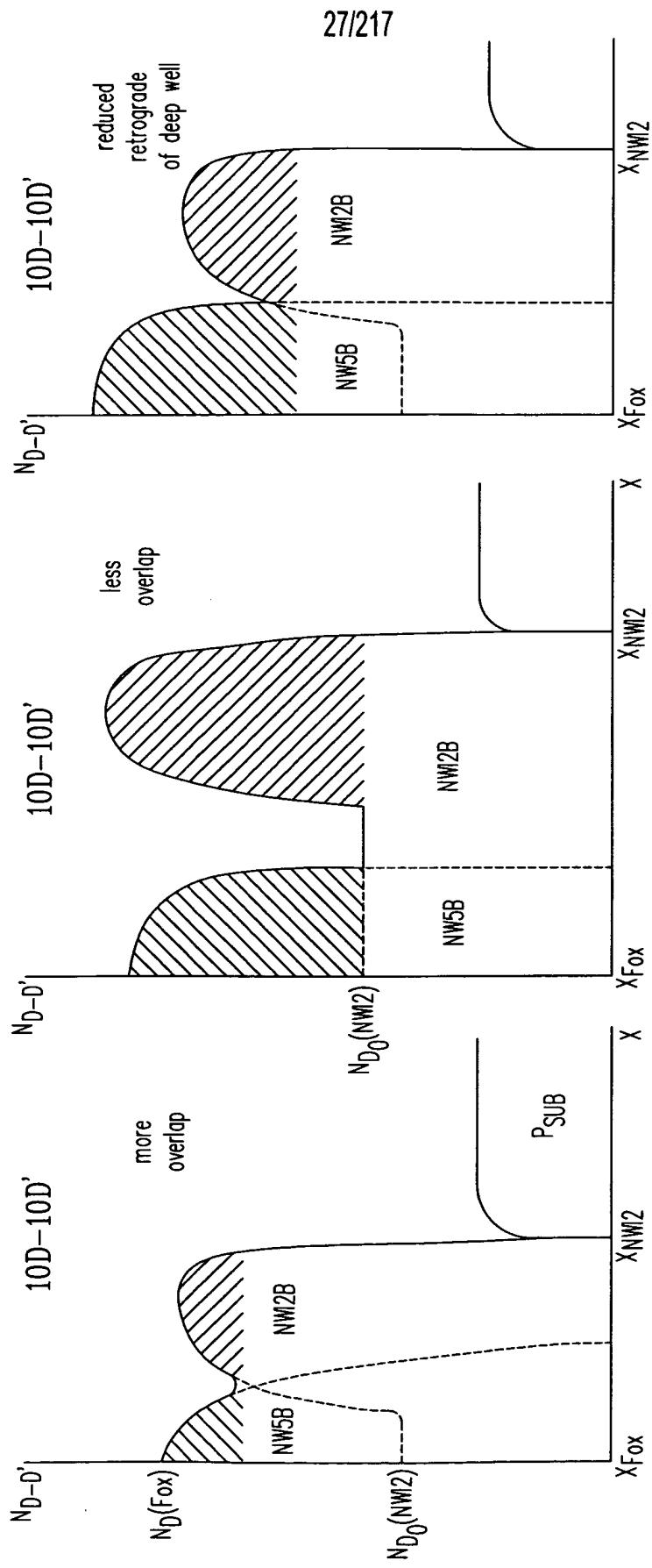


FIG. 10G

FIG. 10H

FIG. 10I

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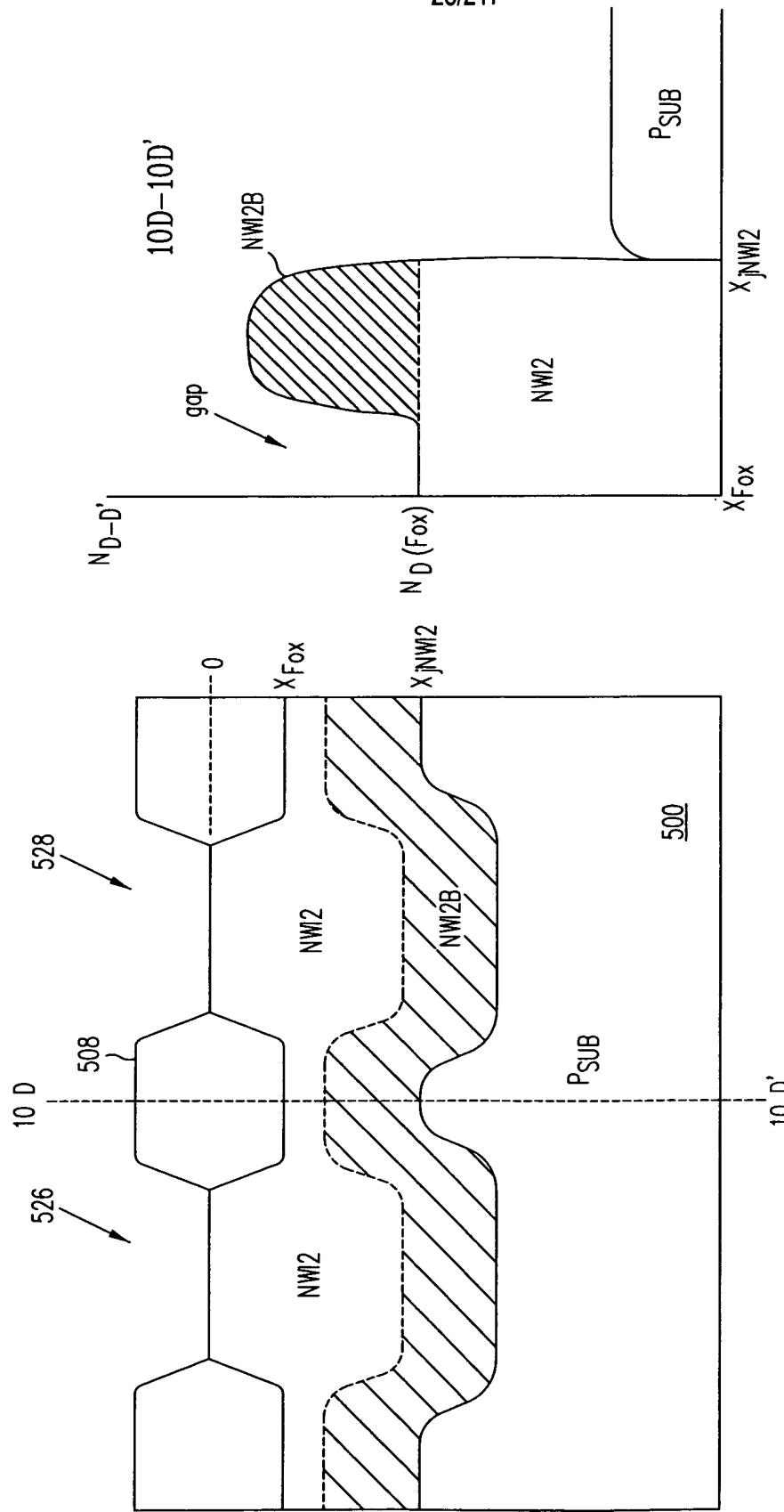


FIG. 10K

FIG. 10J

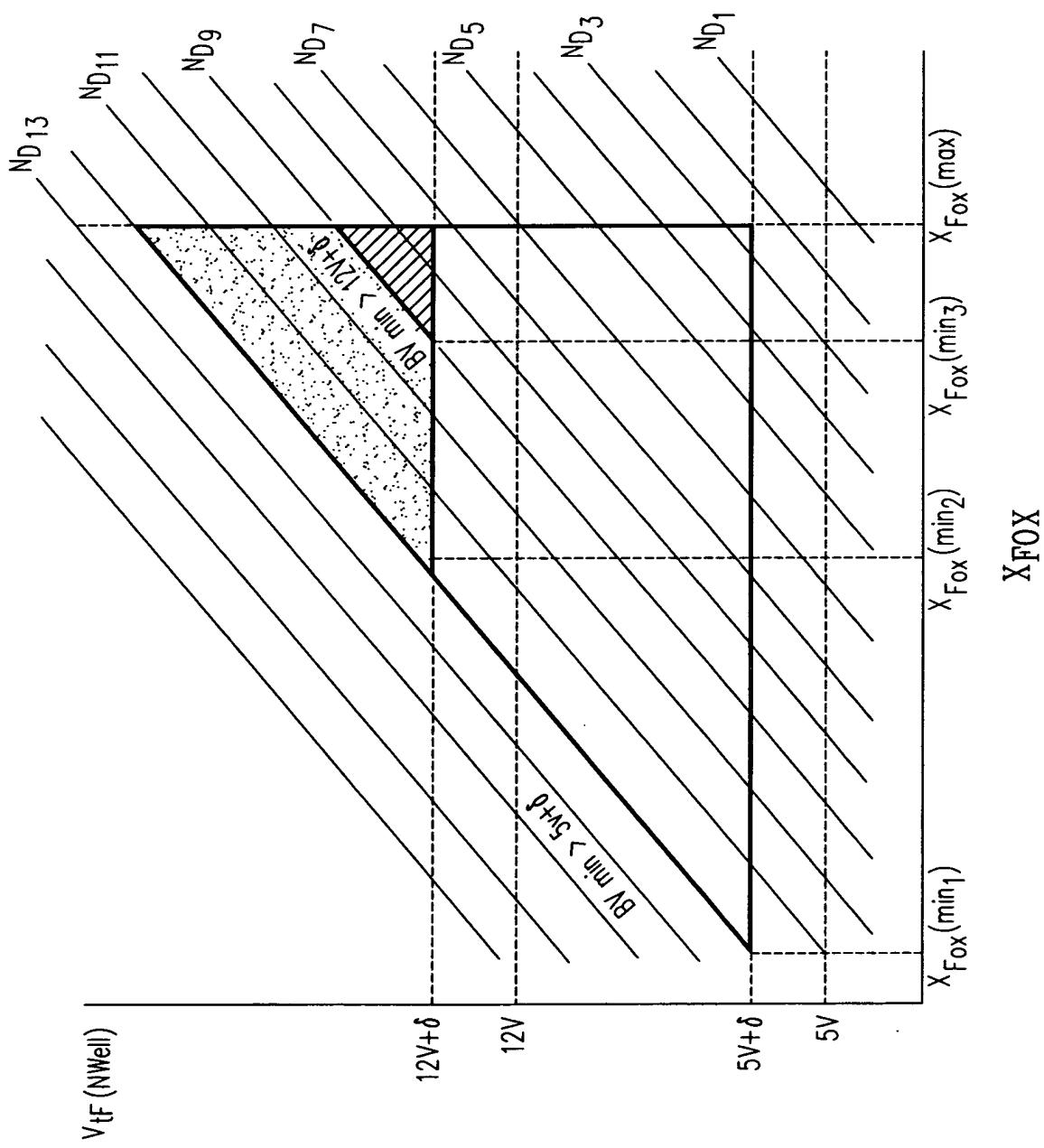


FIG. 10L

X_{FOX}

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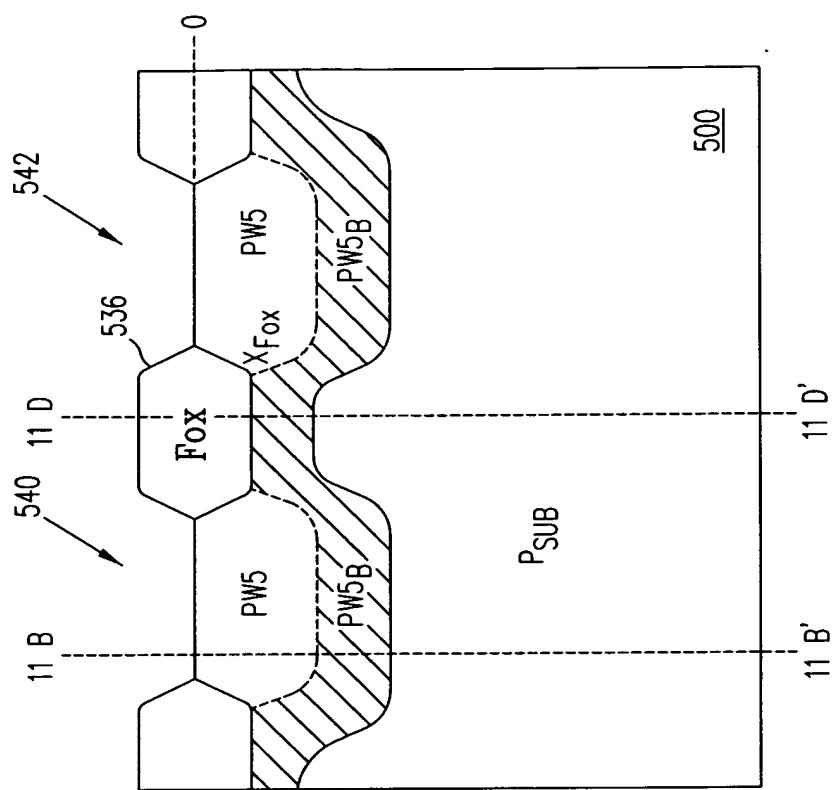


FIG. 11B

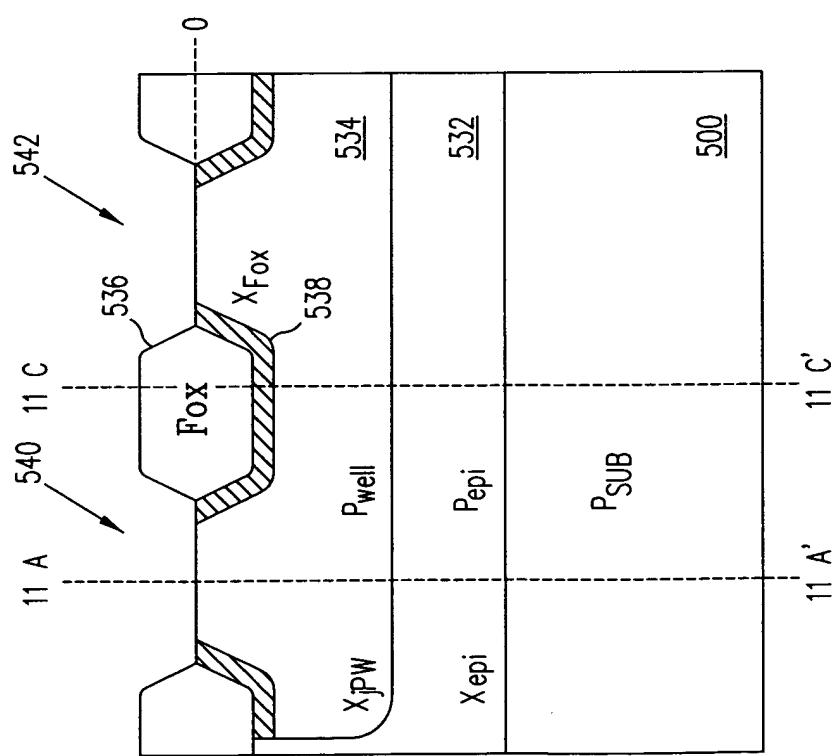


FIG. 11A

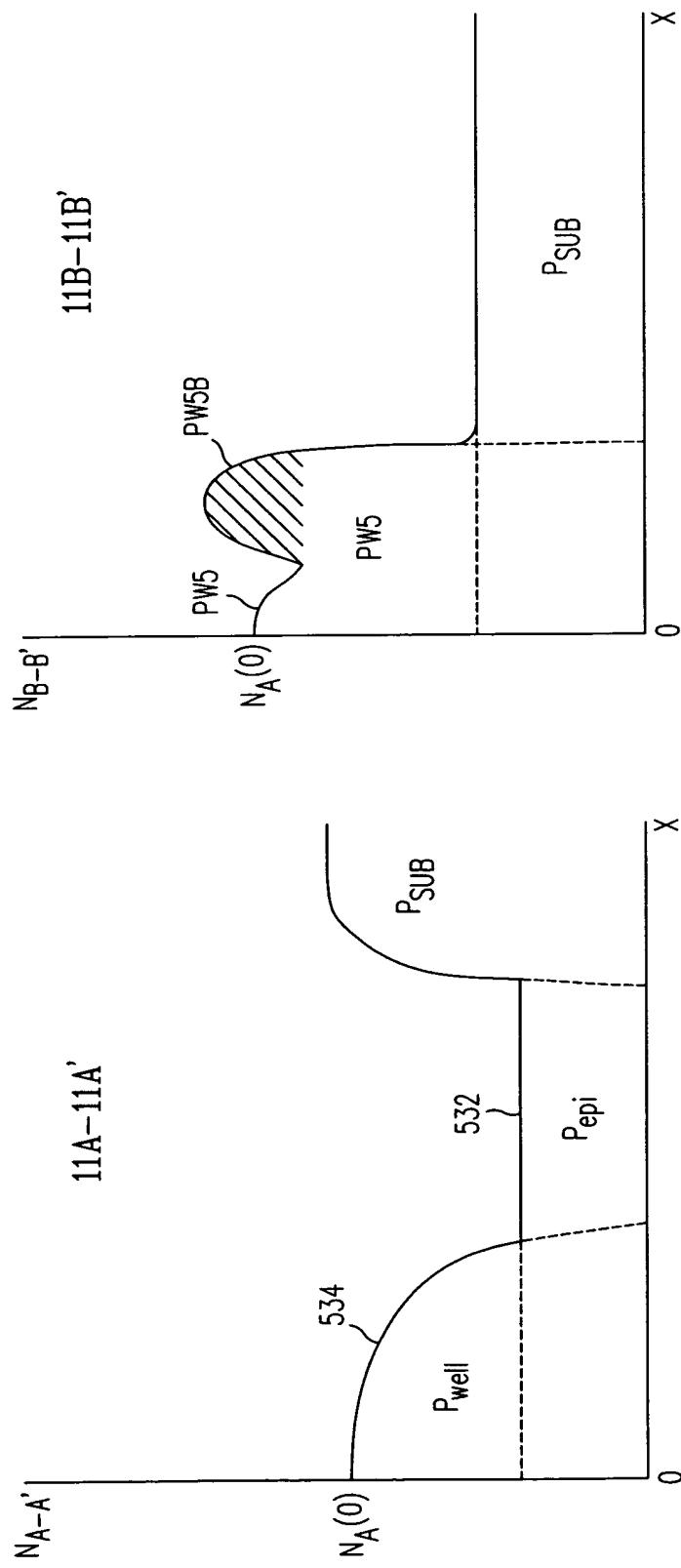


FIG. 11D

FIG. 11C

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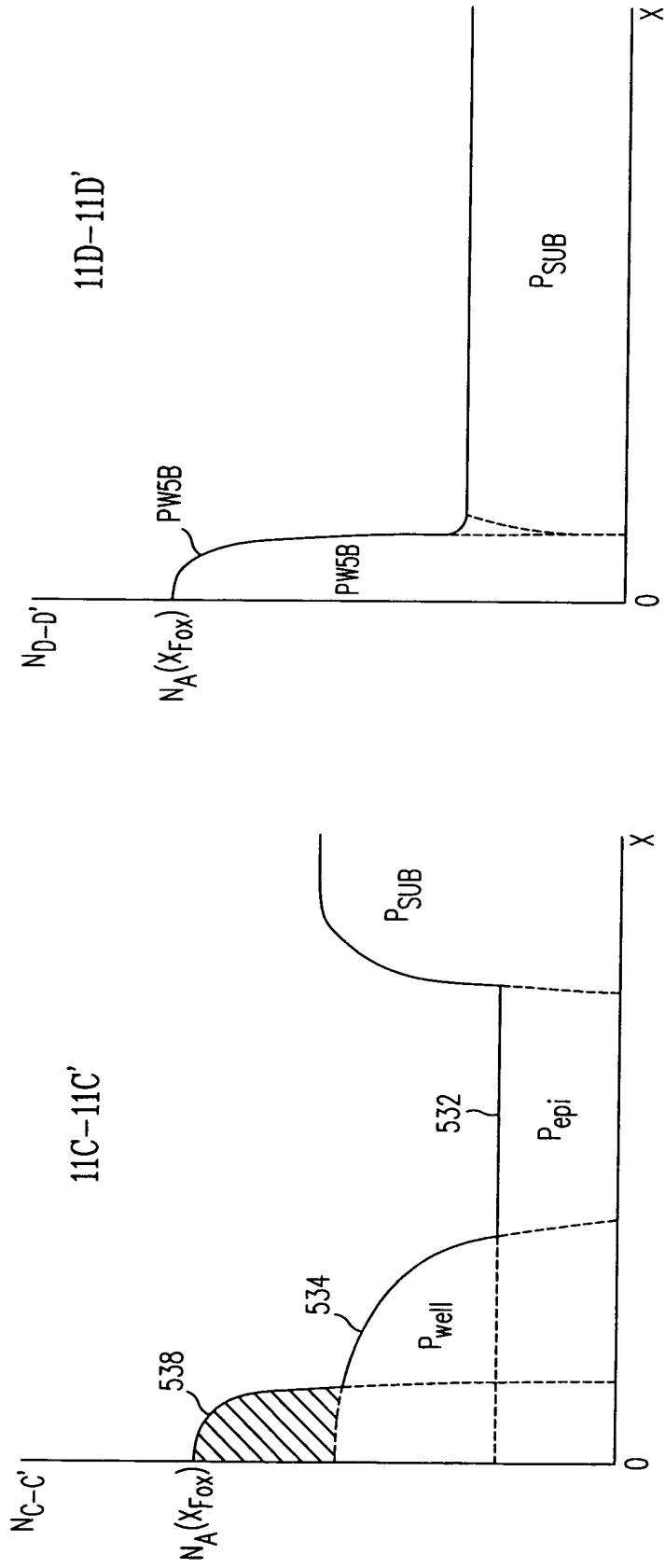


FIG. 11F

FIG. 11E

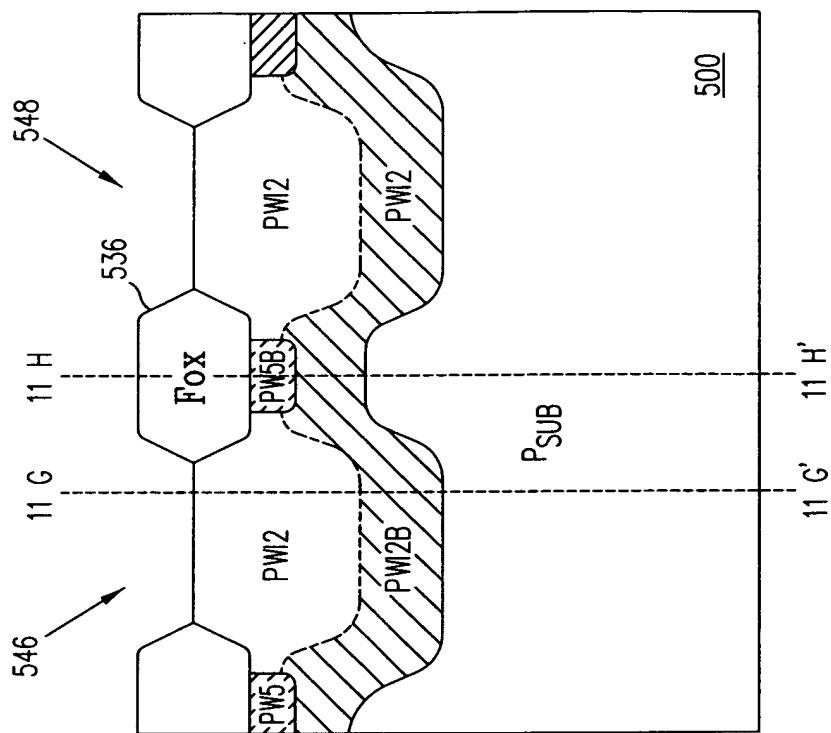


FIG. 11H

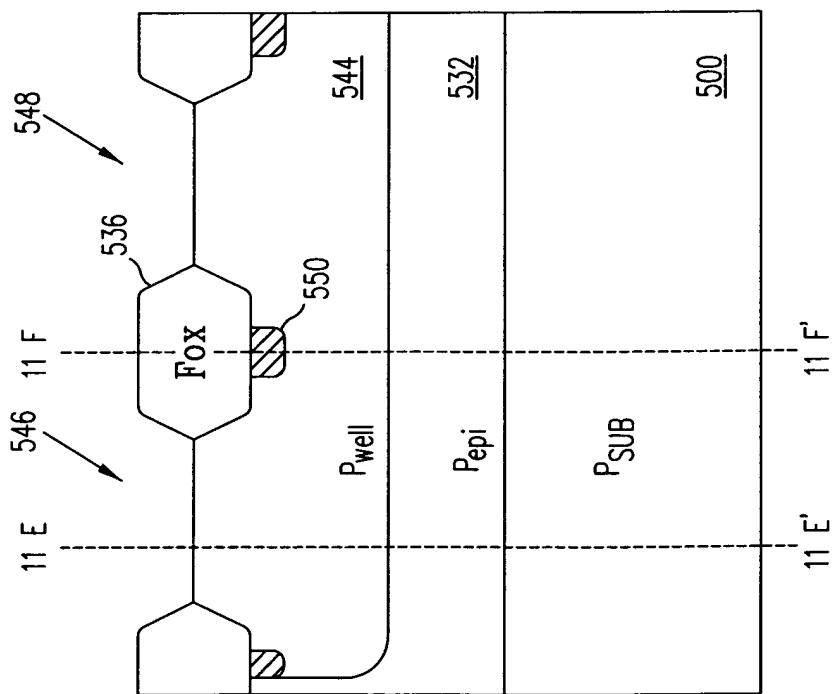


FIG. 11G

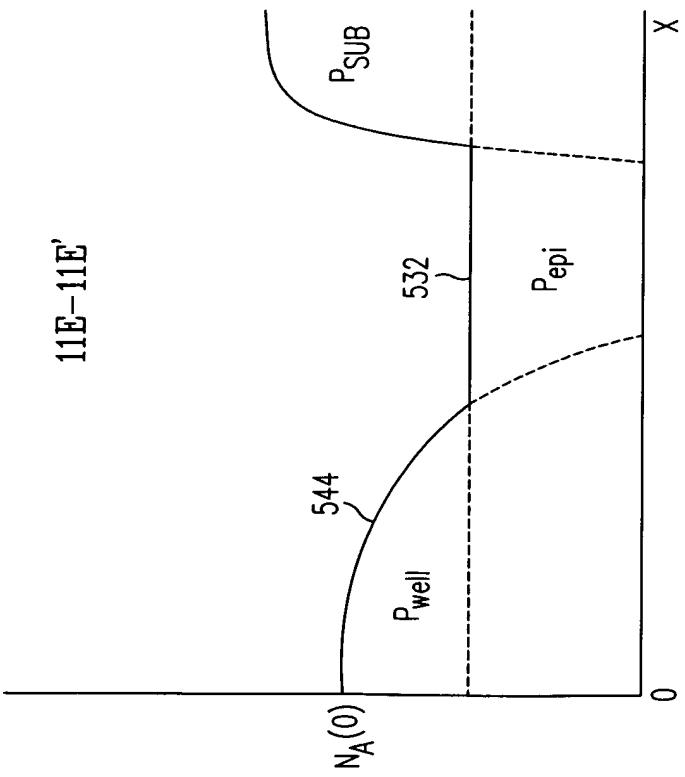
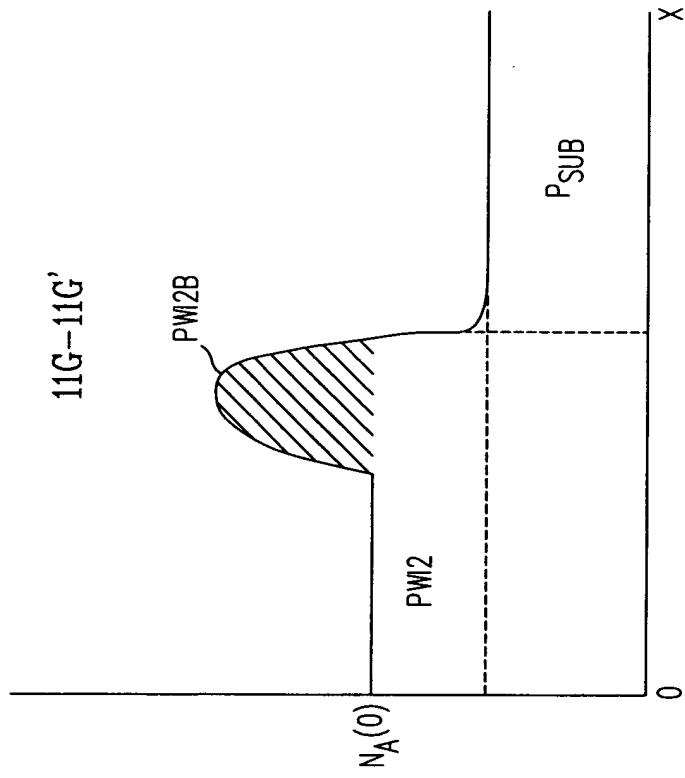


FIG. 11J

FIG. 11I

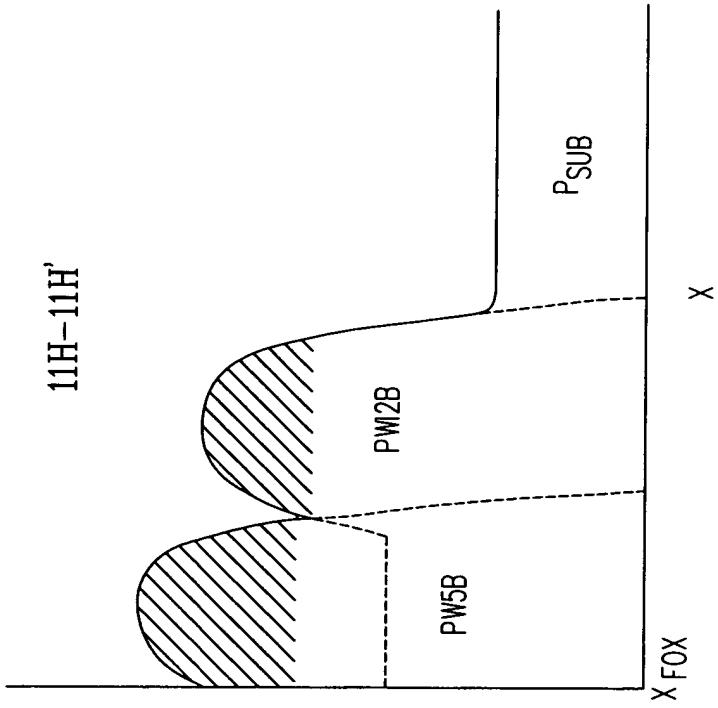


FIG. 11L

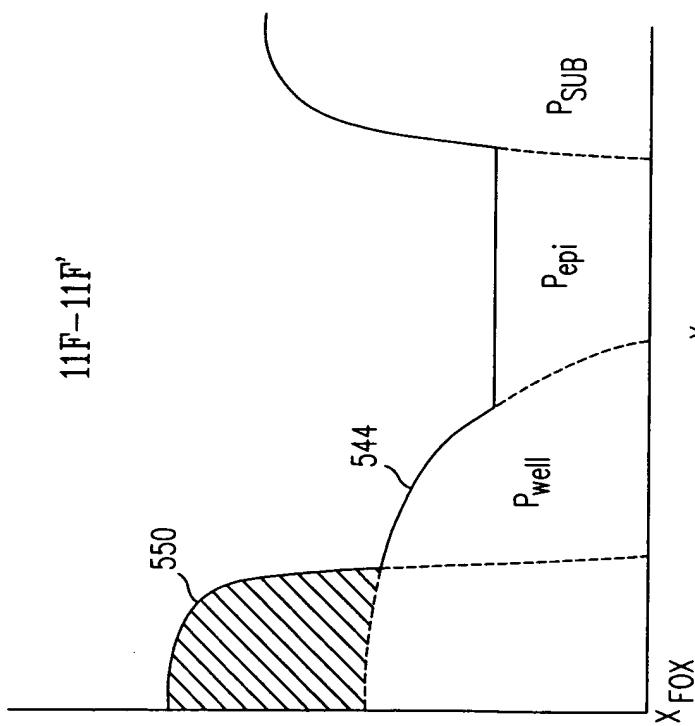


FIG. 11K

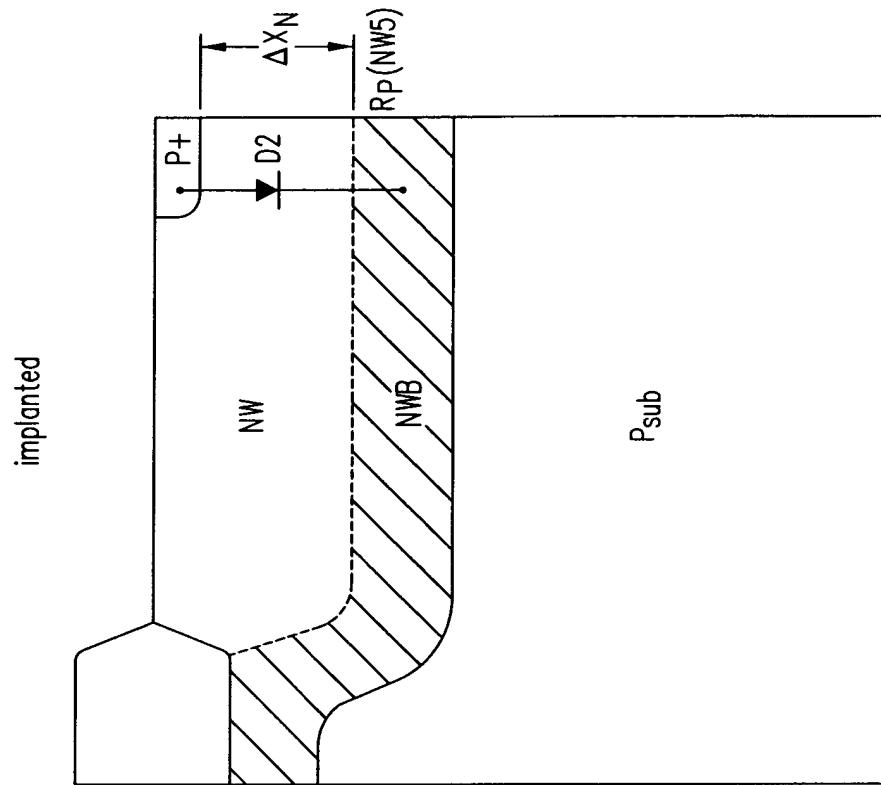


FIG. 12B

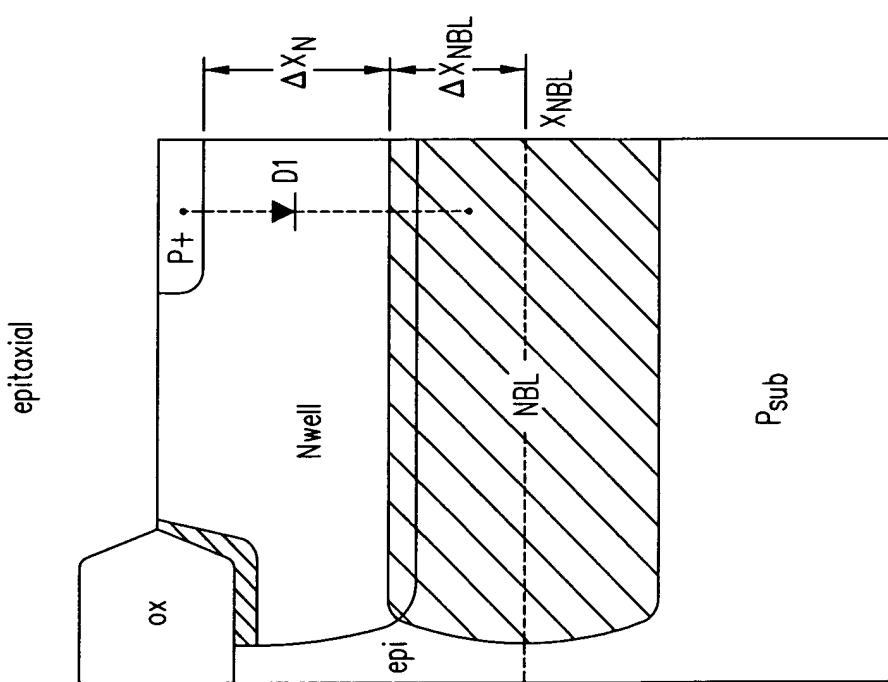


FIG. 12A

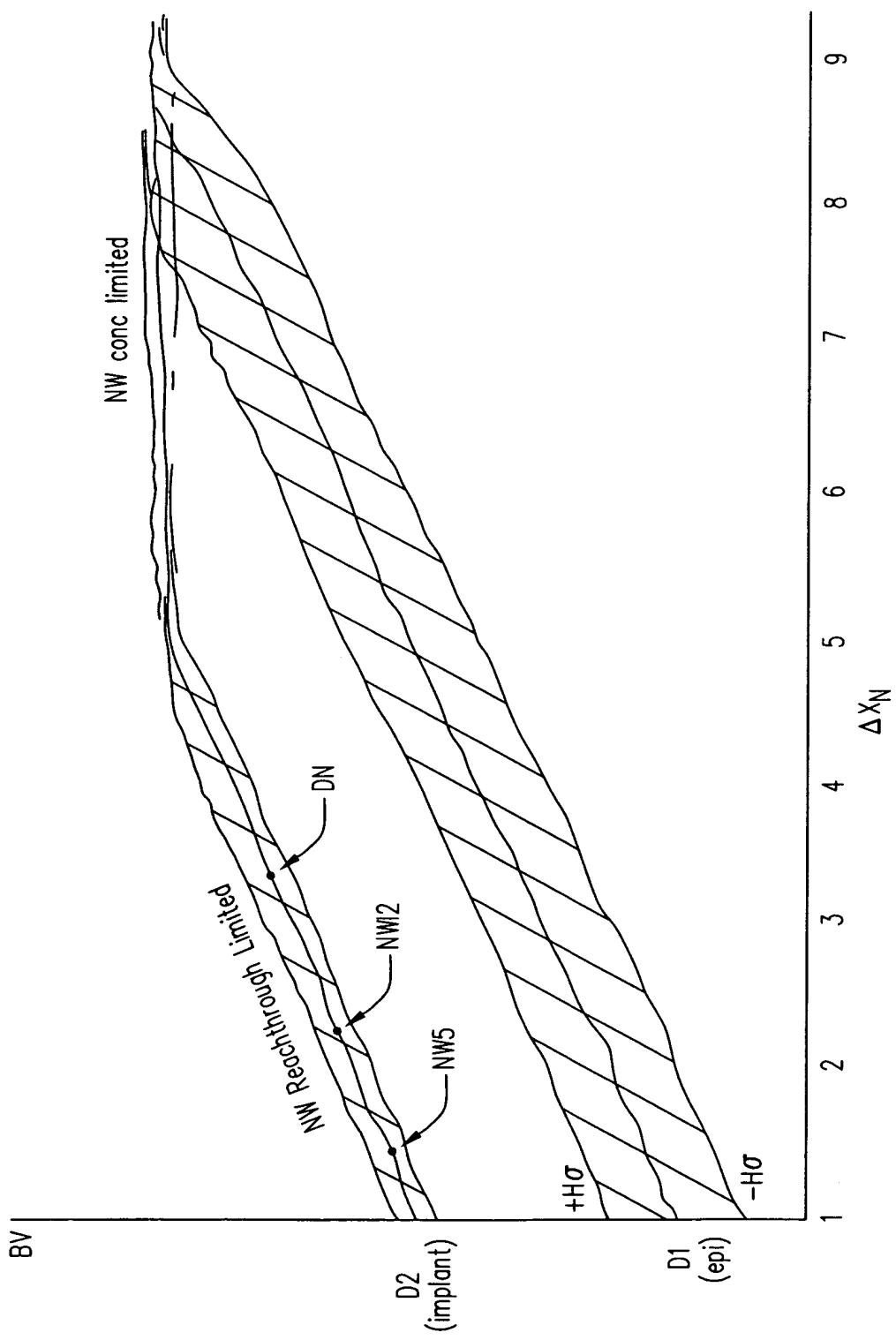


FIG. 12C

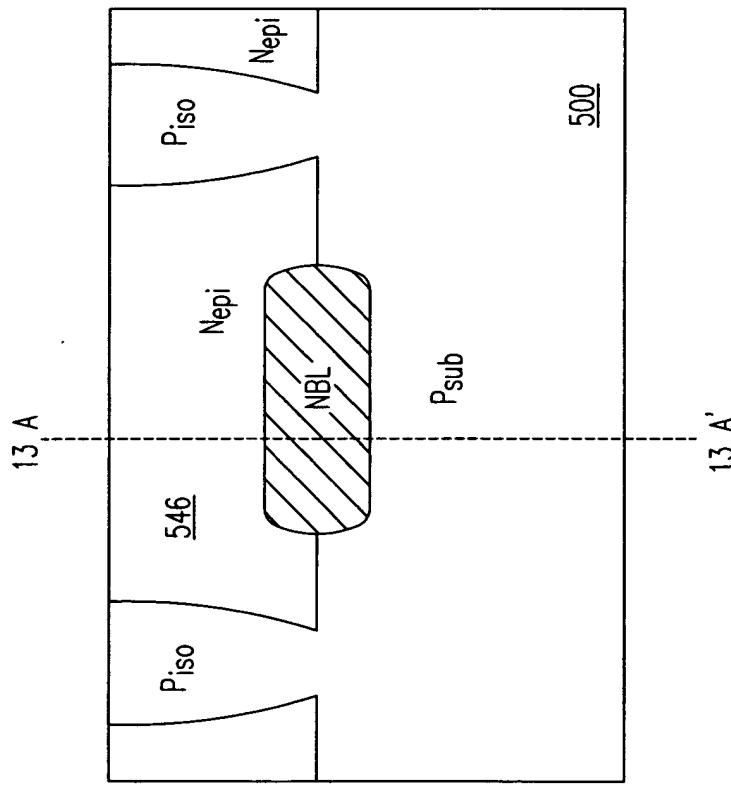


FIG. 13A
(Prior Art)

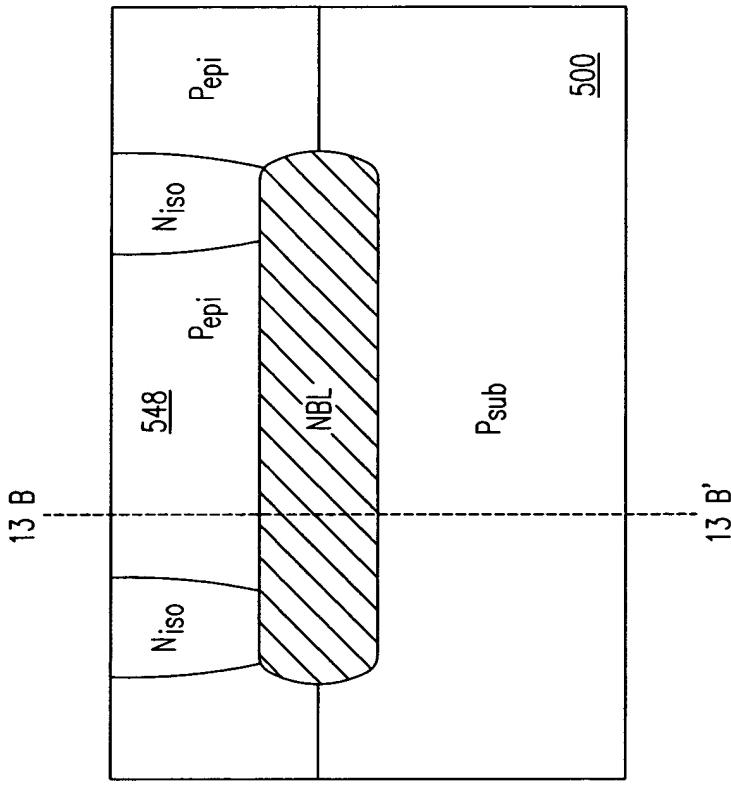


FIG. 13B
(Prior Art)

13B-13B'

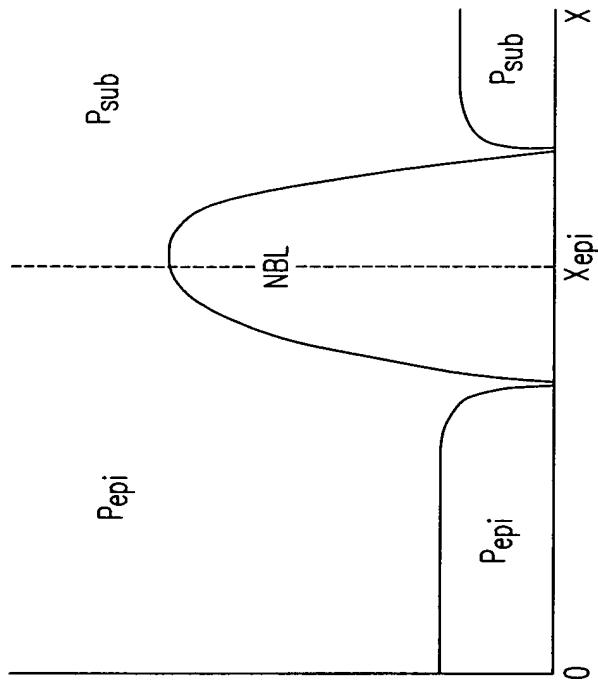


FIG. 13D

13A-13A'

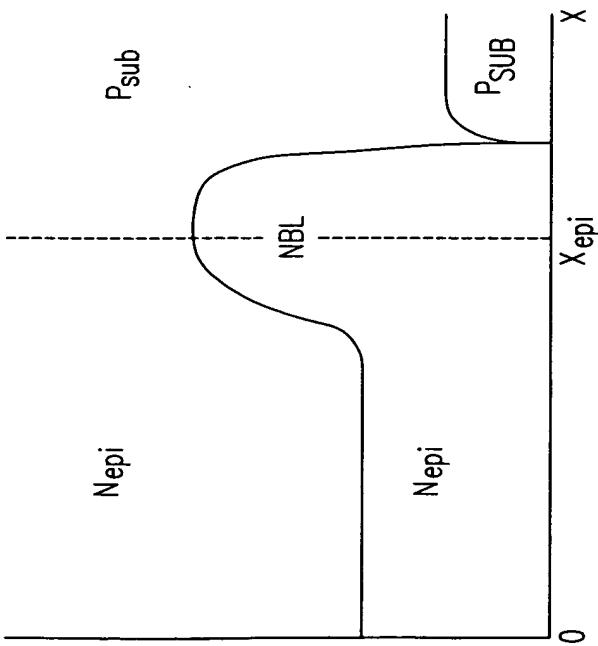


FIG. 13C

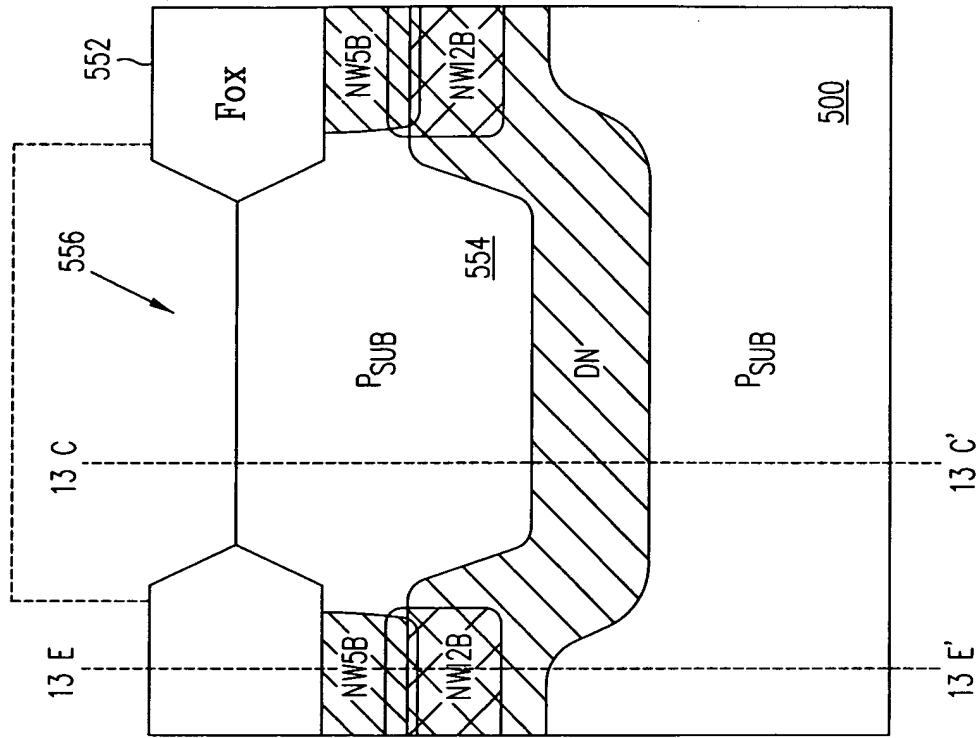


FIG. 13F

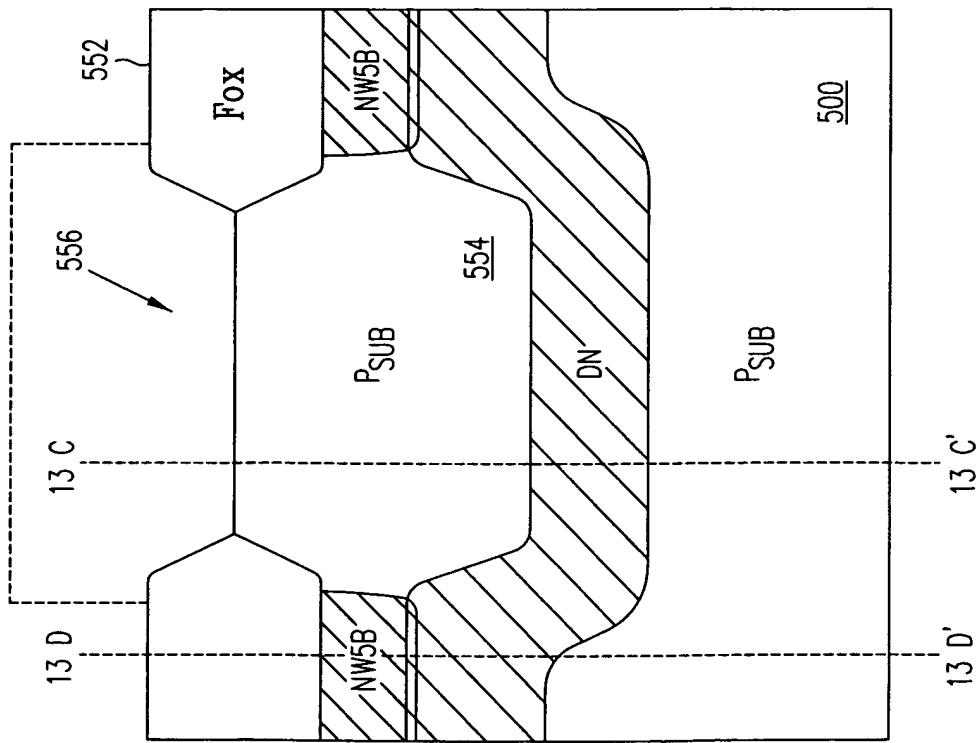


FIG. 13E

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13D-13D'
13C-13C'

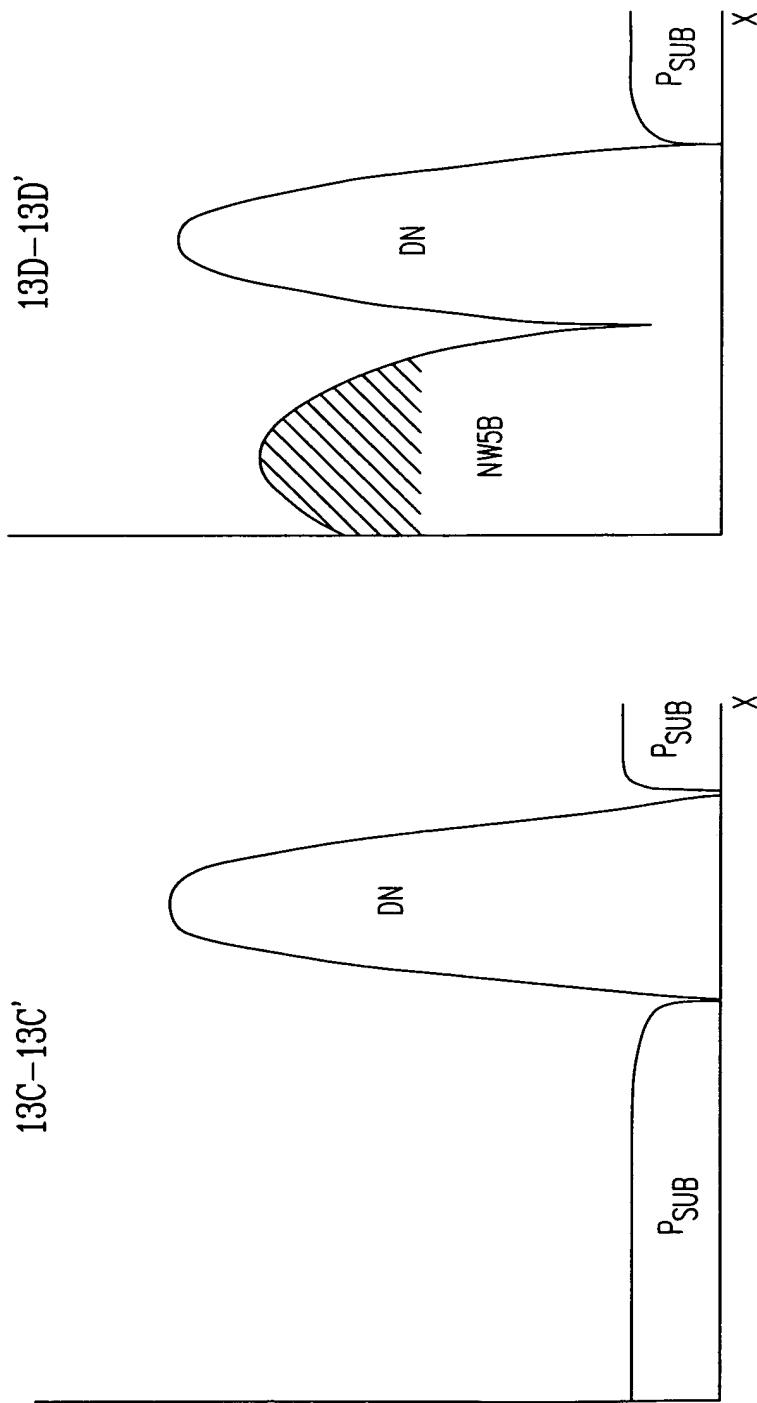


FIG. 13G

FIG. 13H

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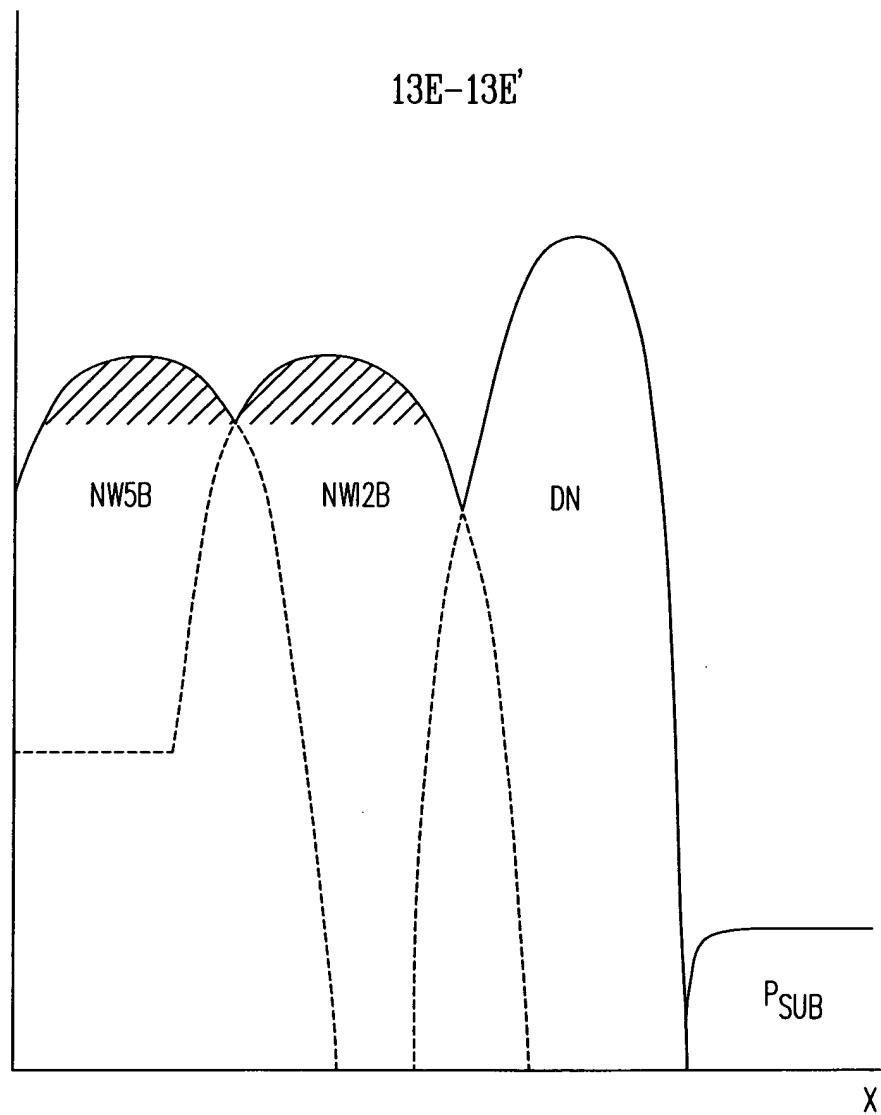


FIG. 13I

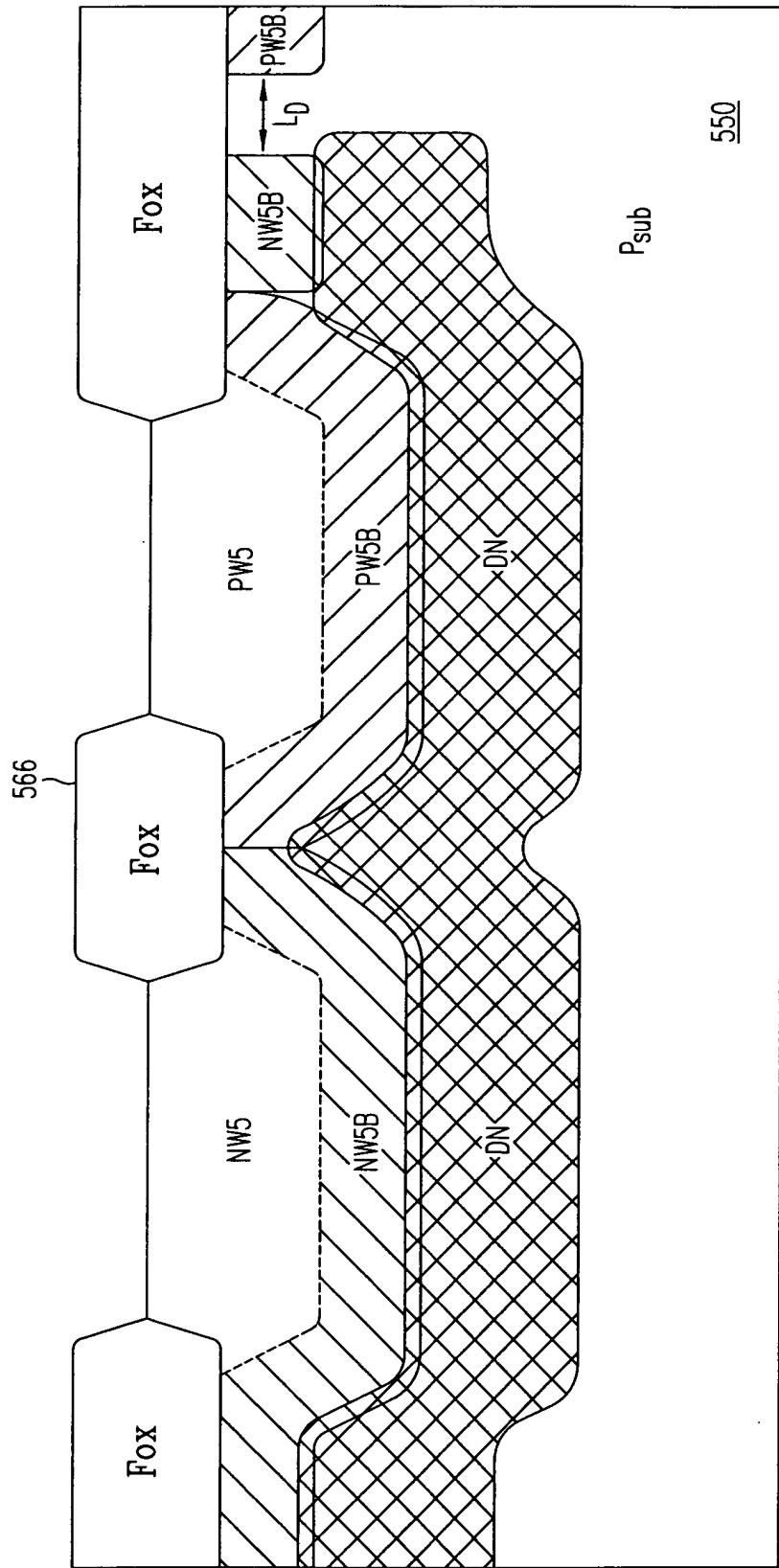


FIG. 14A

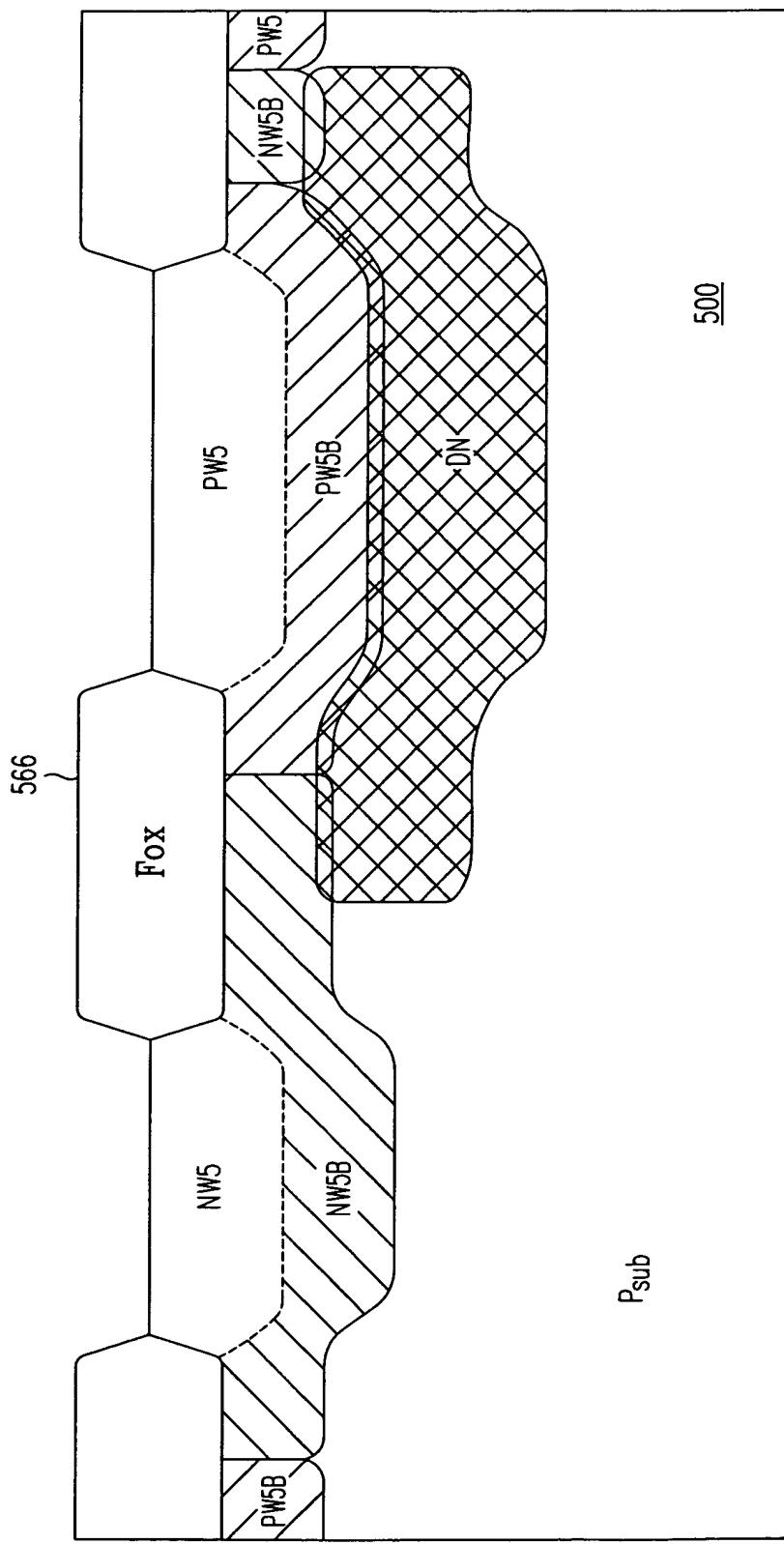


FIG. 14B

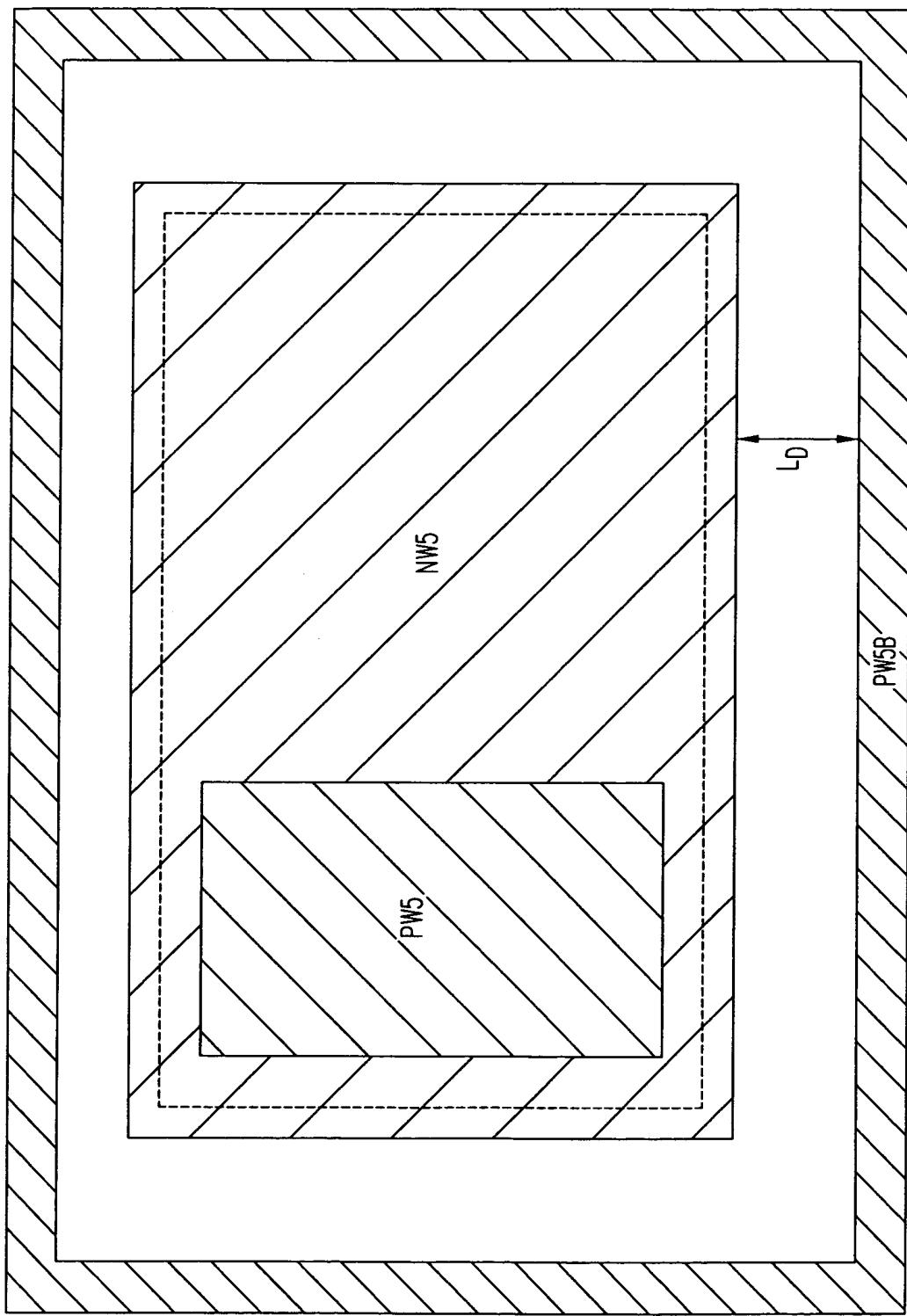


FIG. 14C

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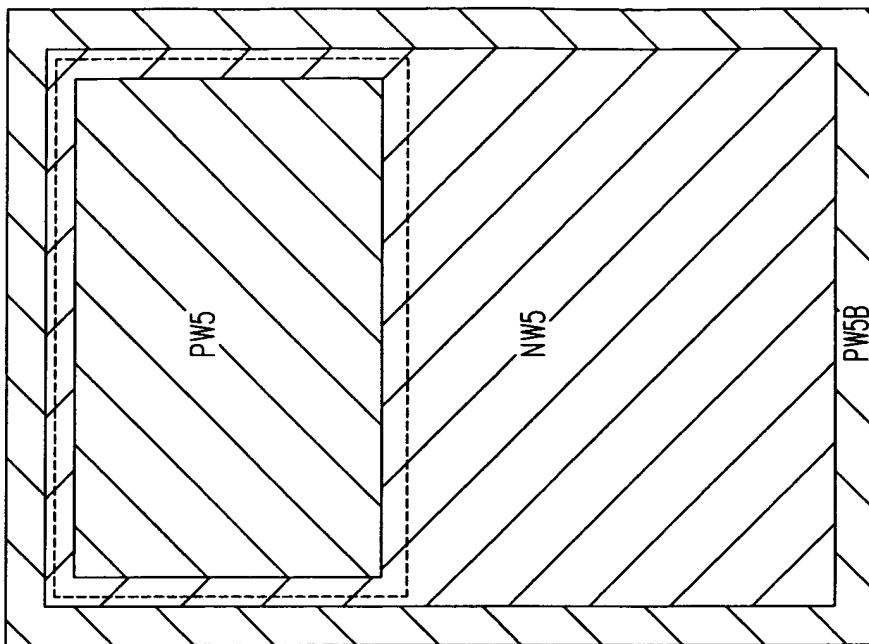


FIG. 14E

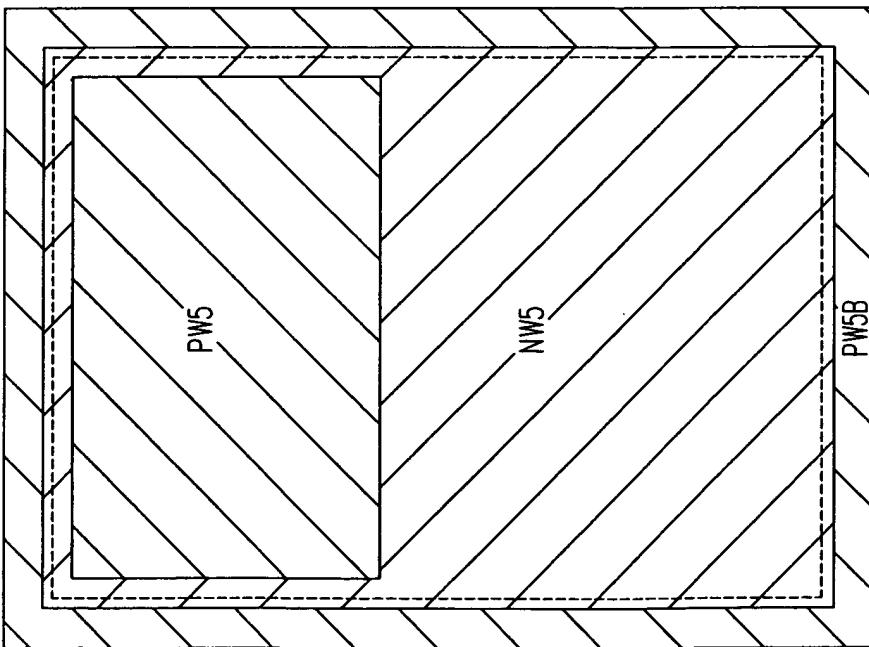


FIG. 14D

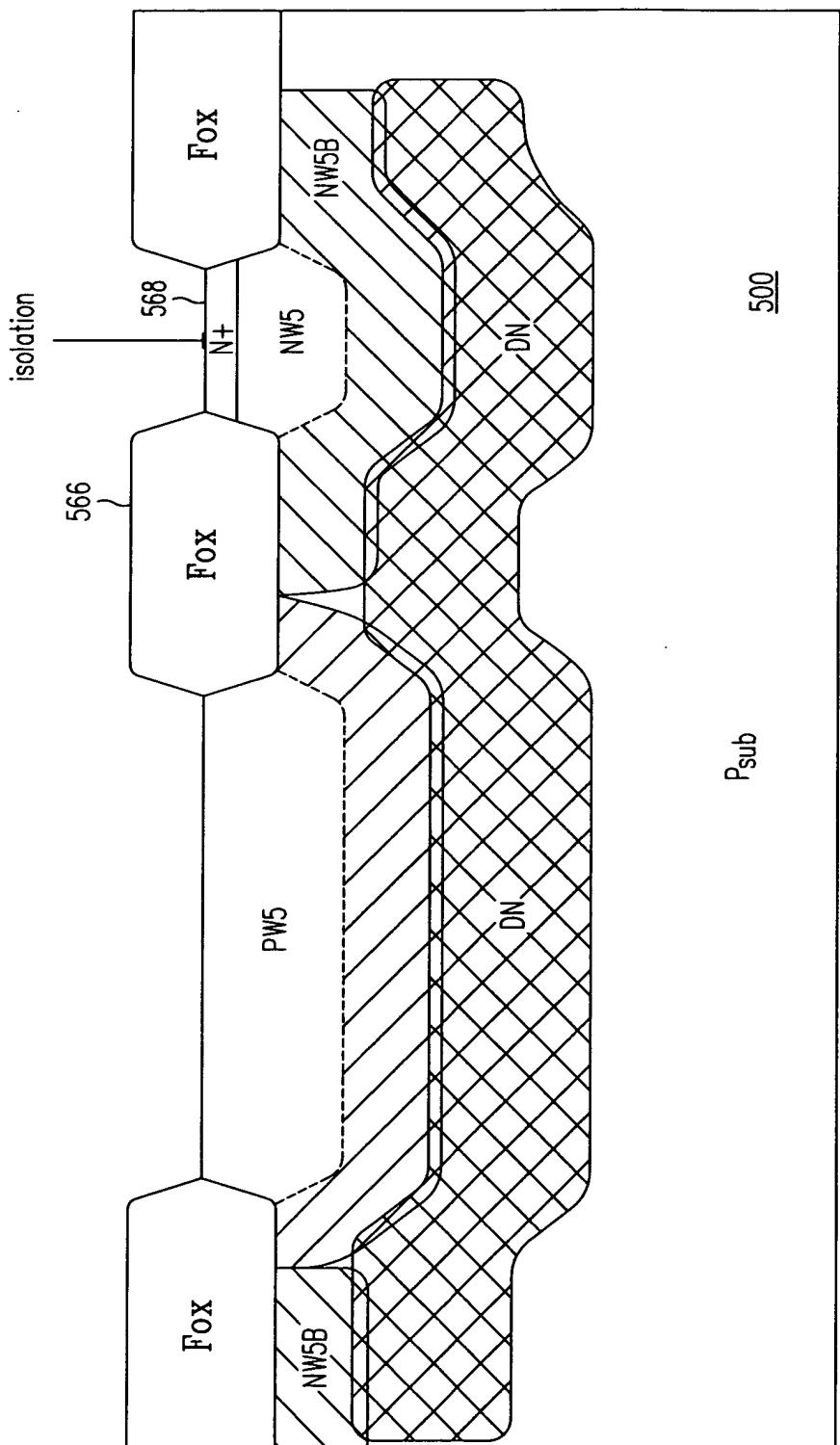


FIG. 14F

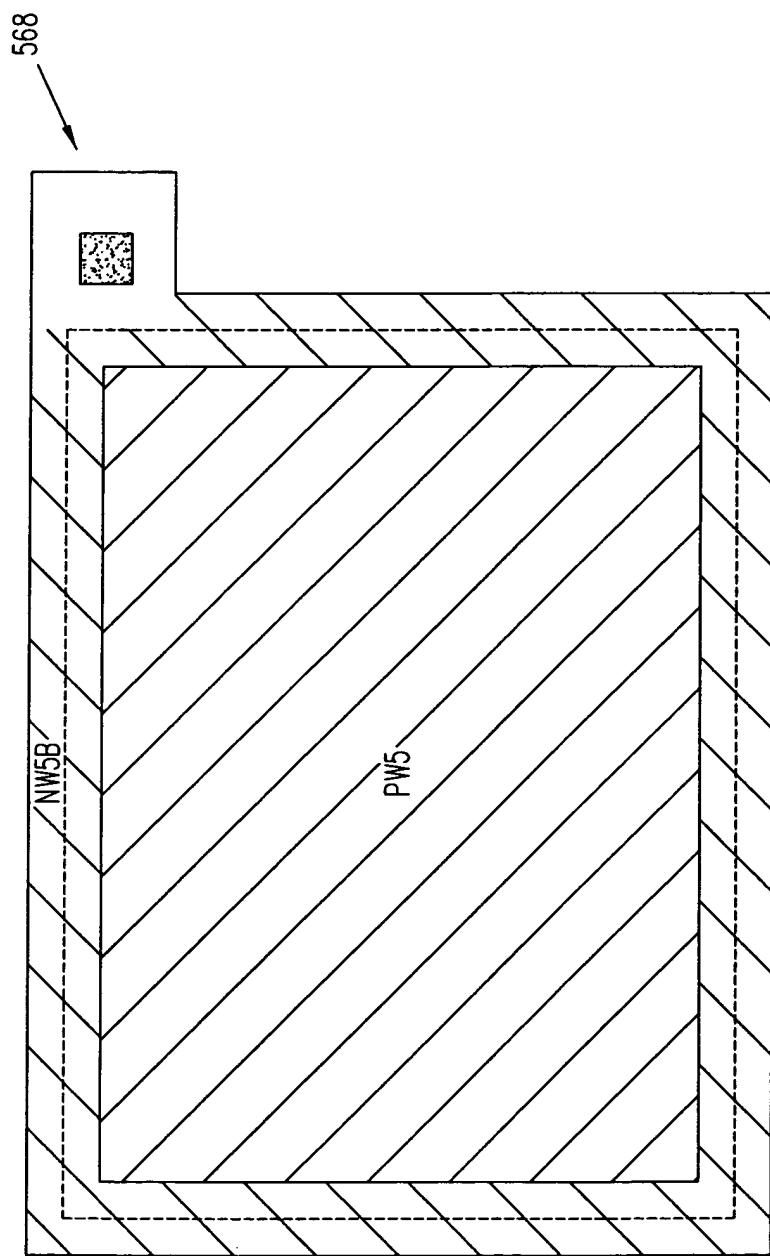


FIG. 14G

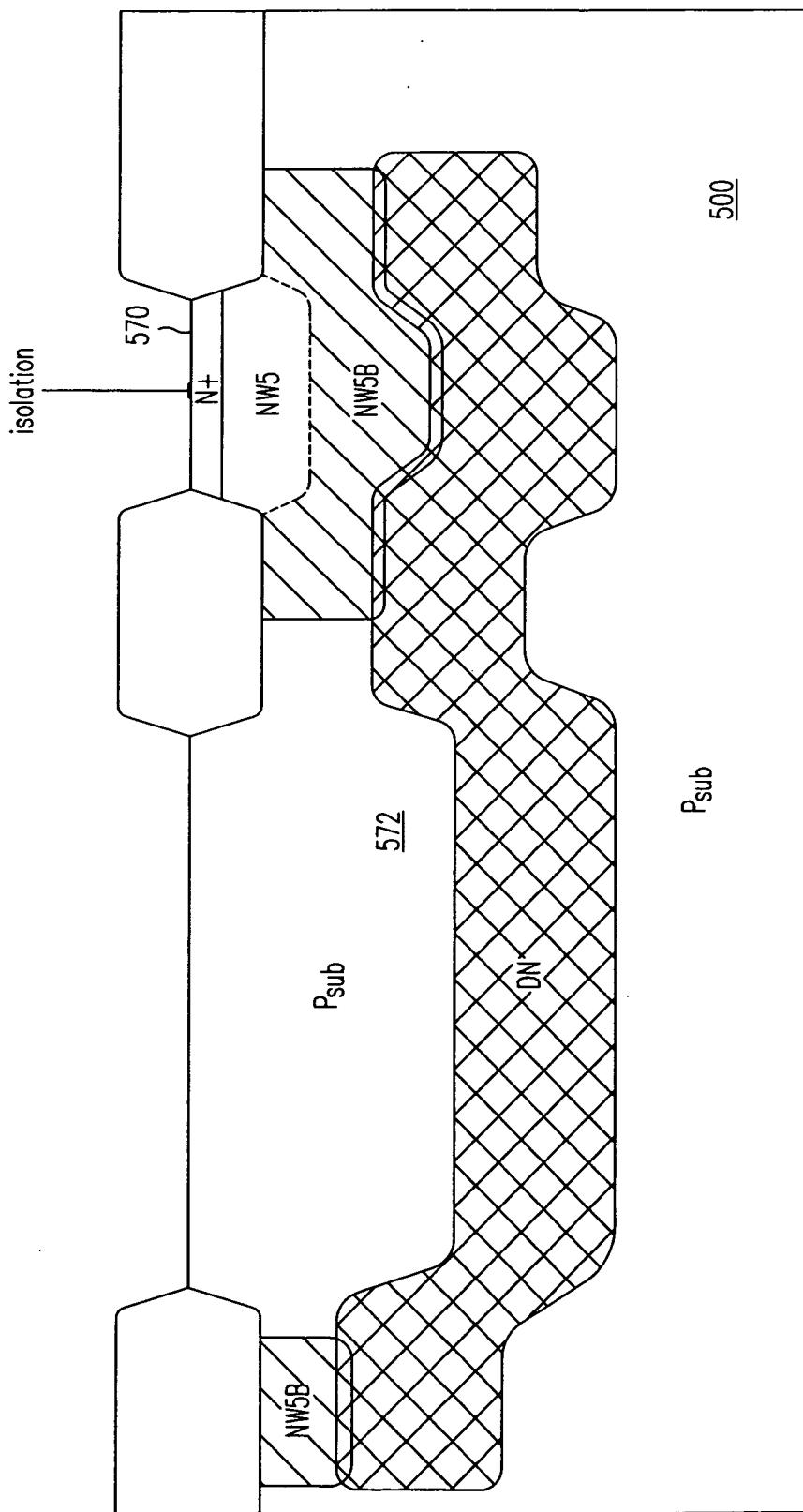


FIG. 14H

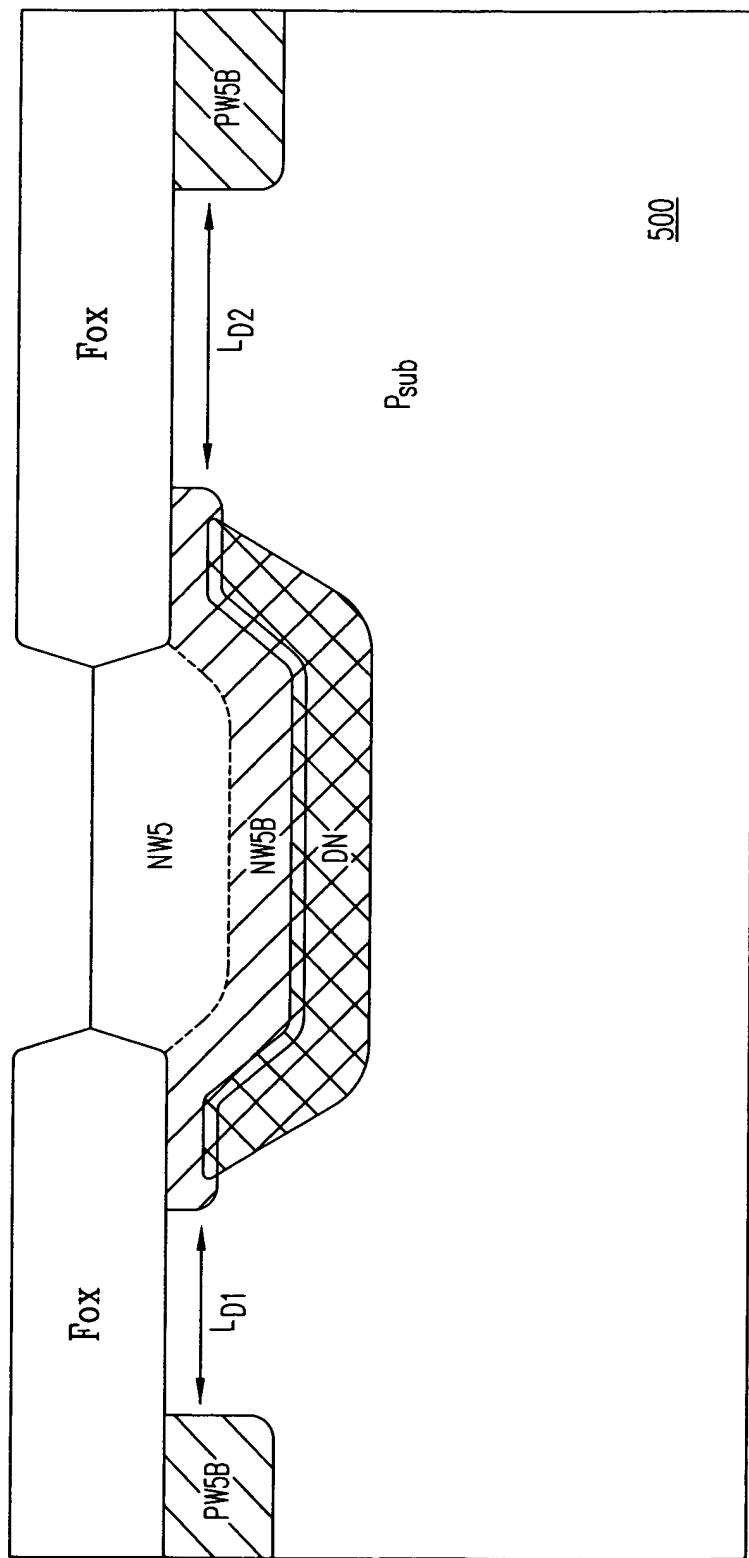


FIG. 14I

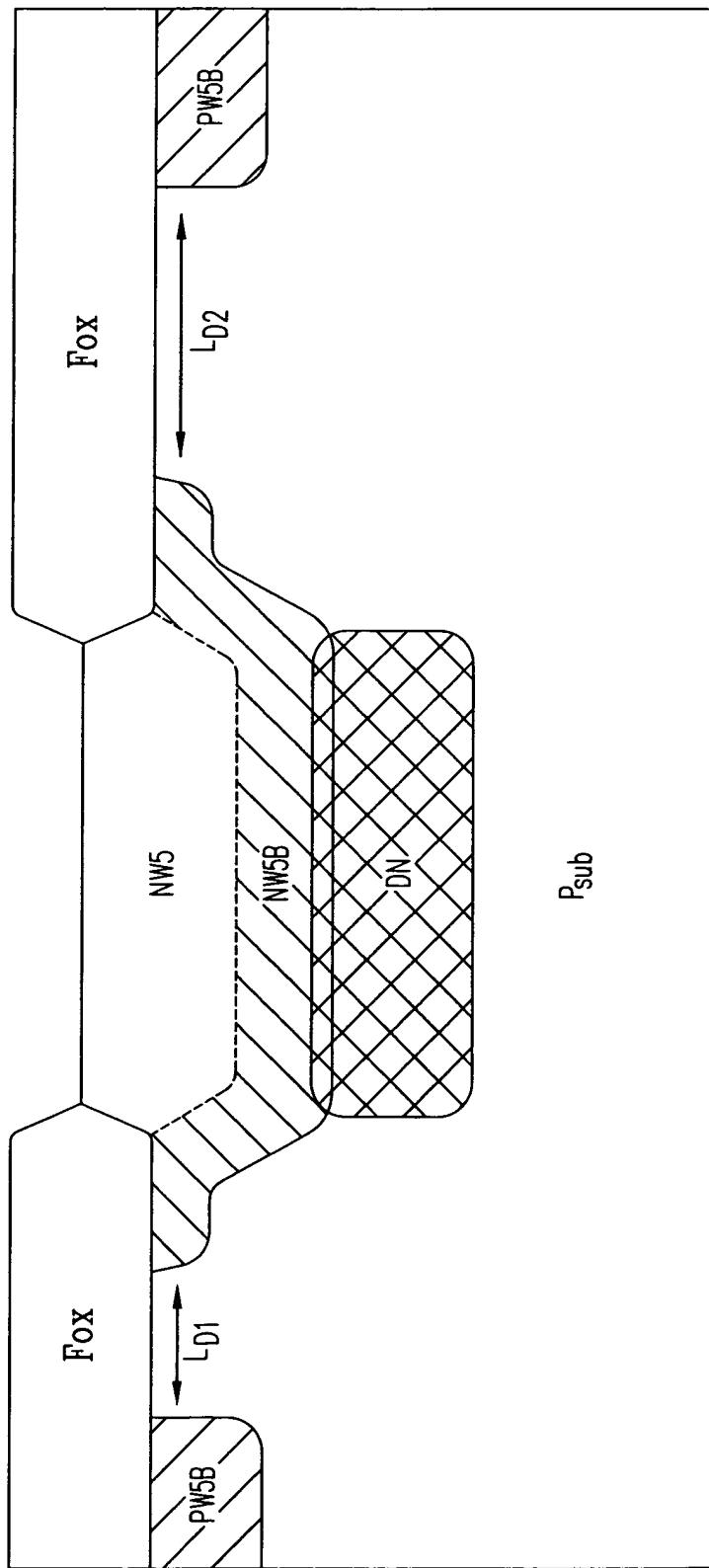


FIG. 14J

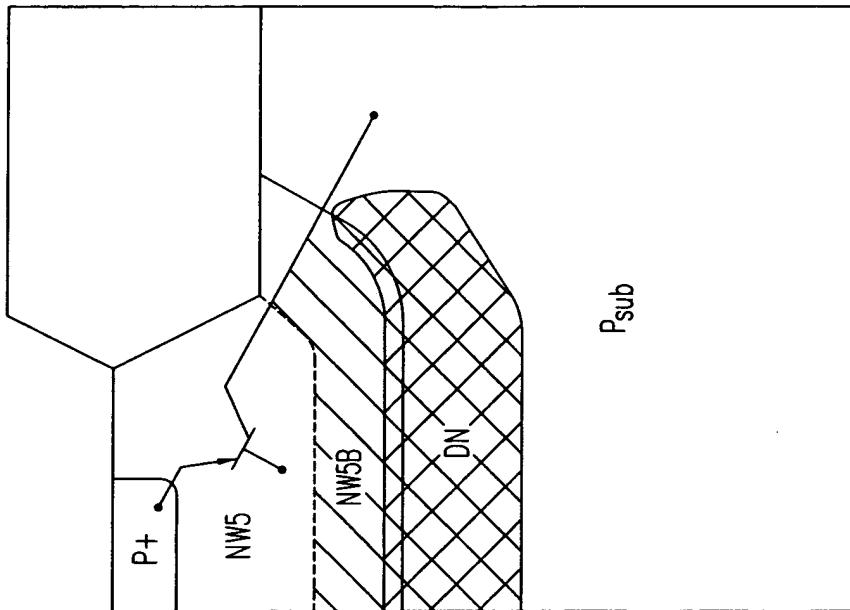


FIG. 14L

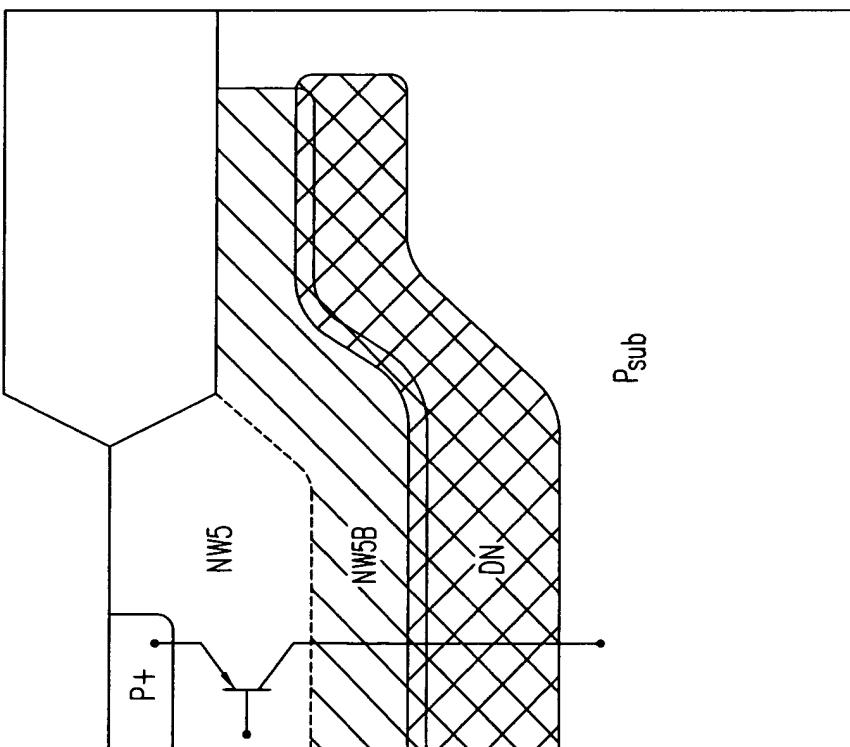


FIG. 14K

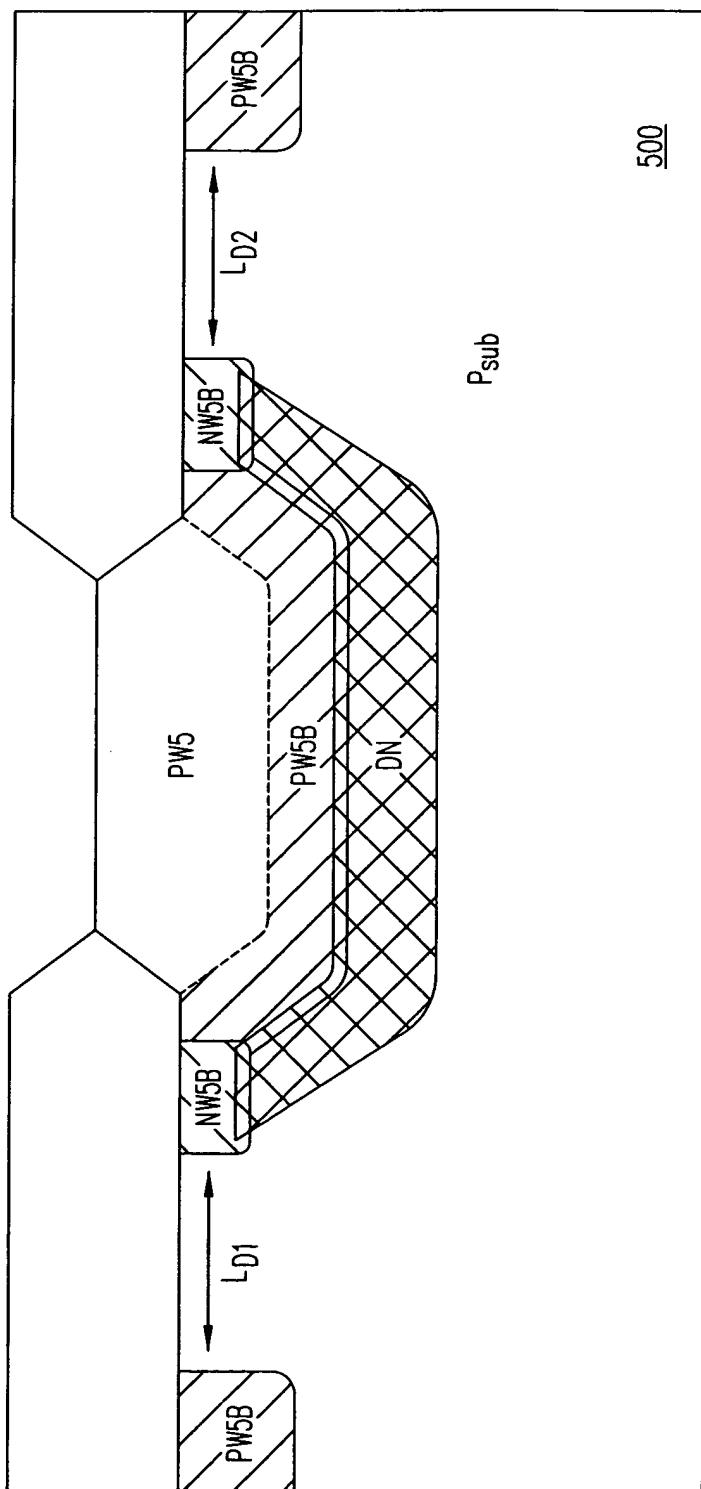


FIG. 14M

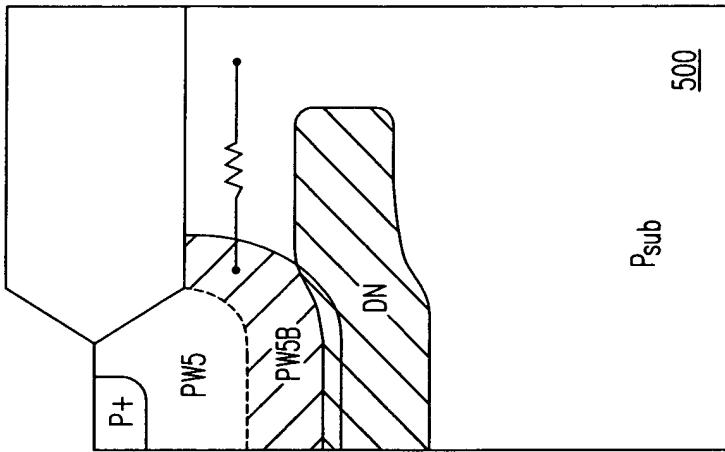


FIG. 14P

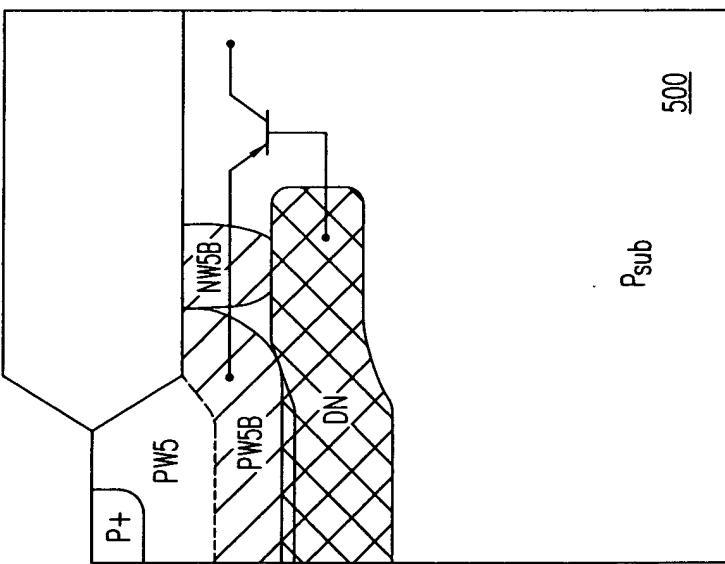


FIG. 14O

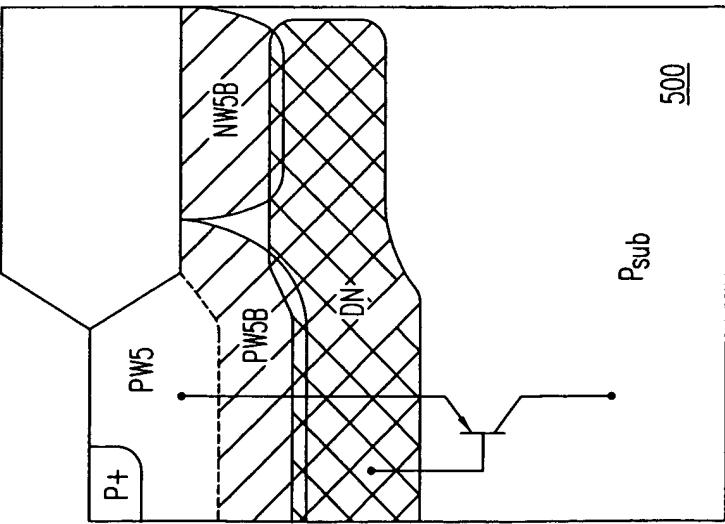


FIG. 14N

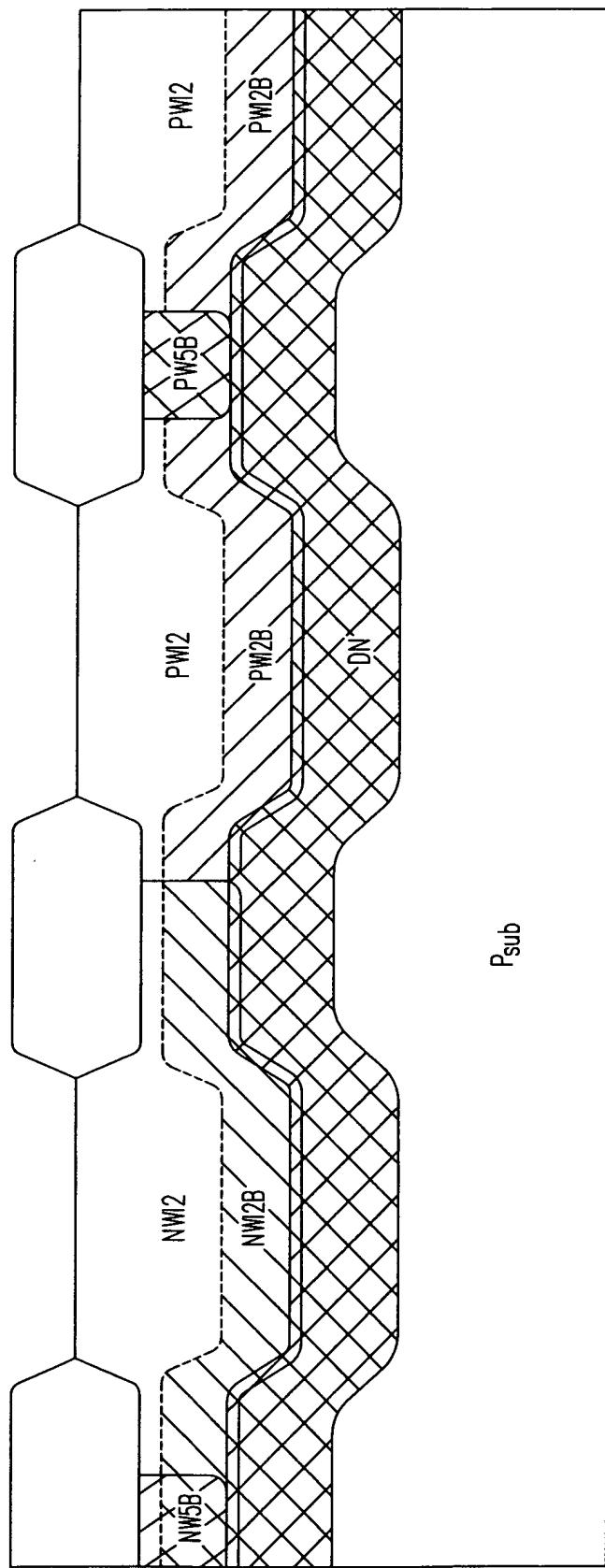


FIG. 15A

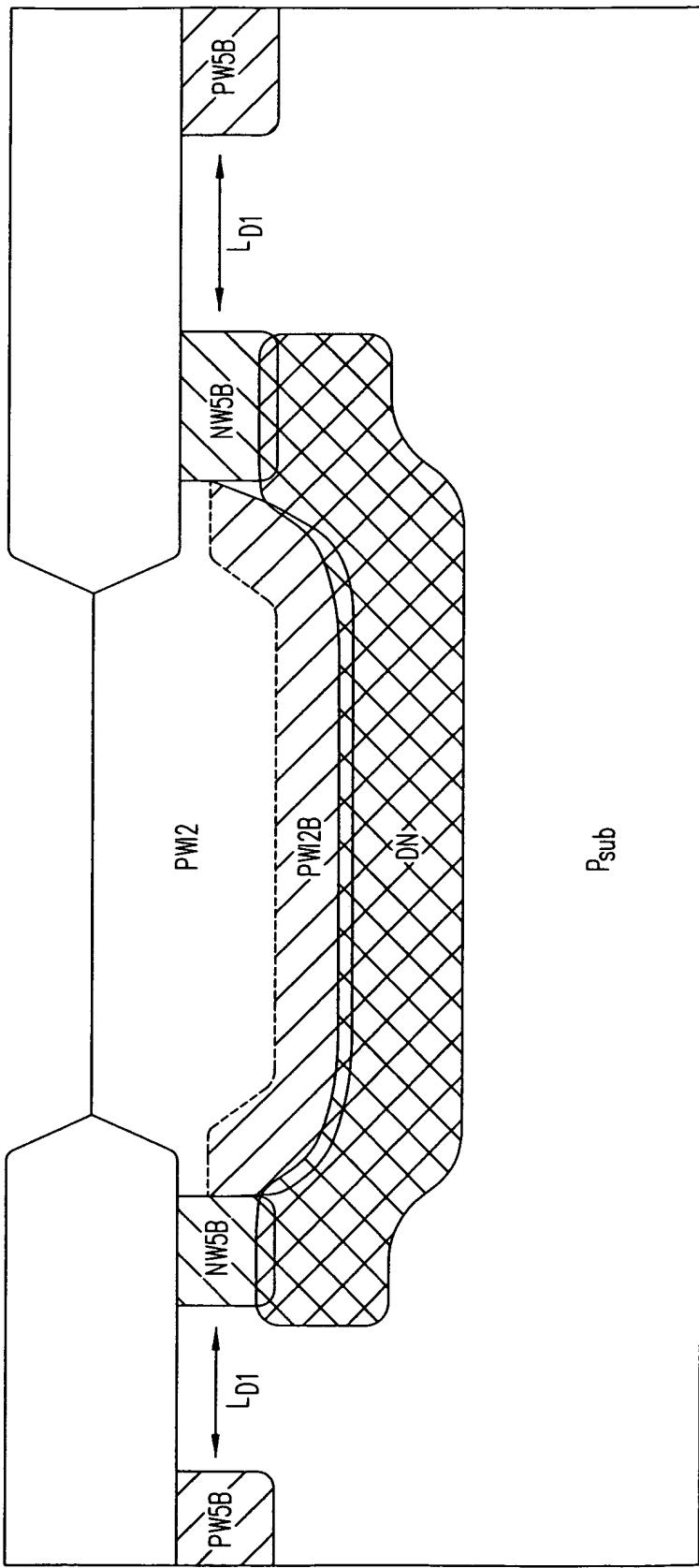


FIG. 15B

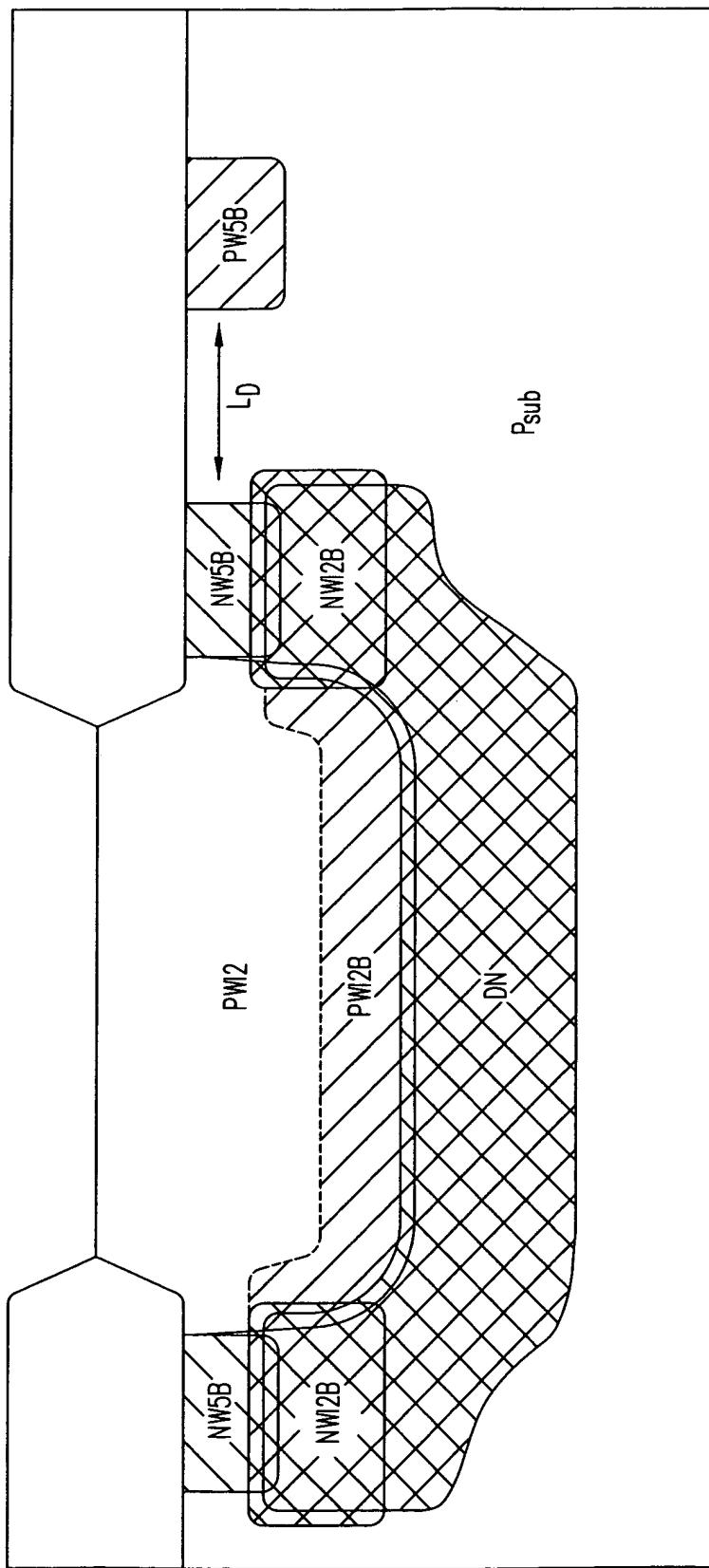


FIG. 15C

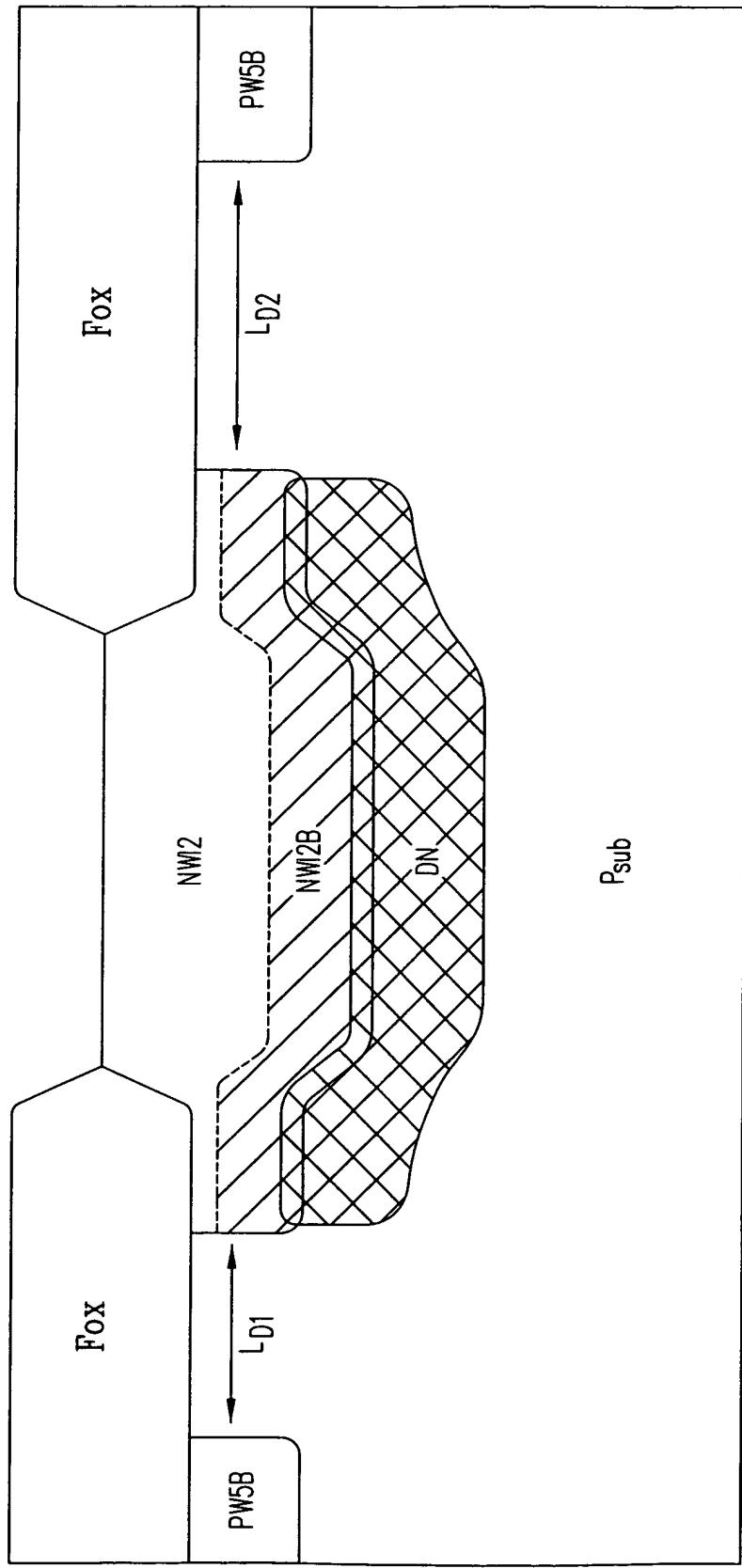


FIG. 15D

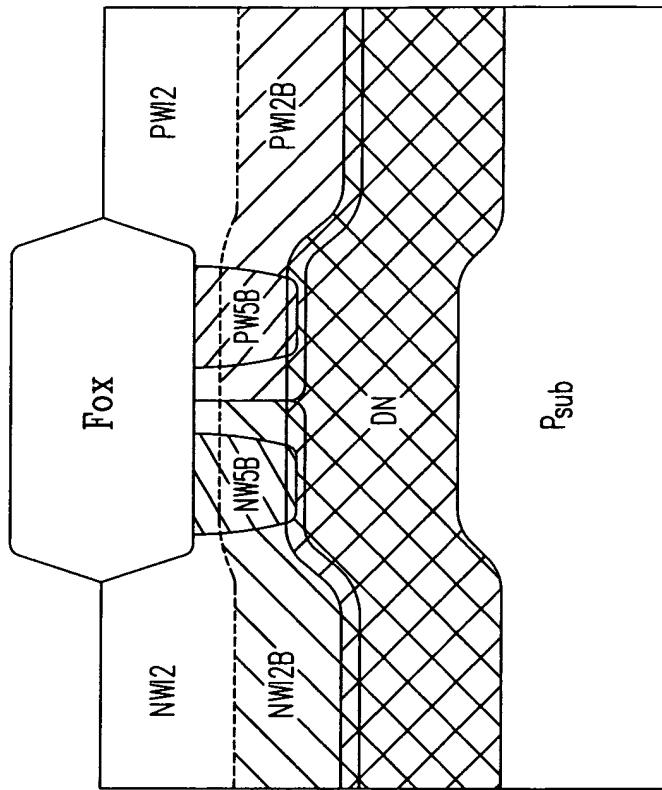


FIG. 15F

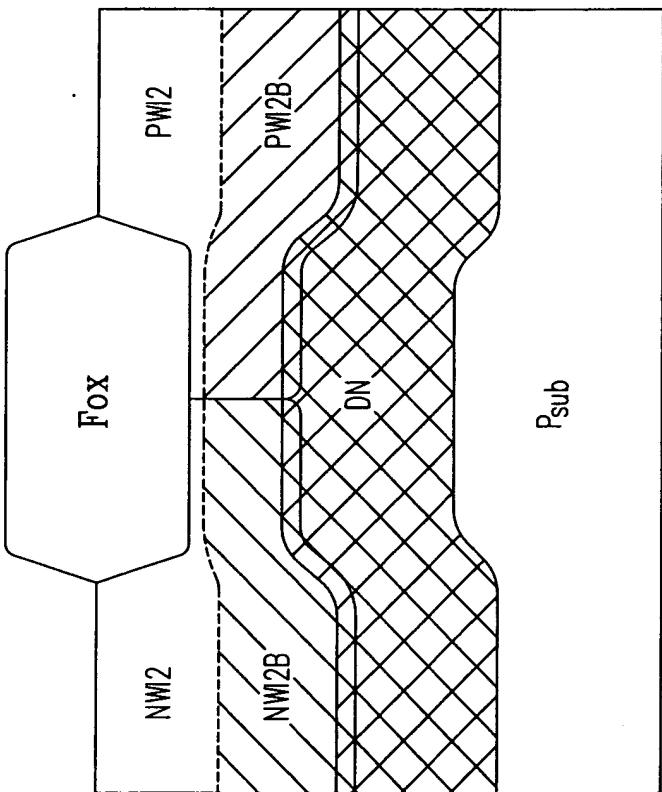


FIG. 15E

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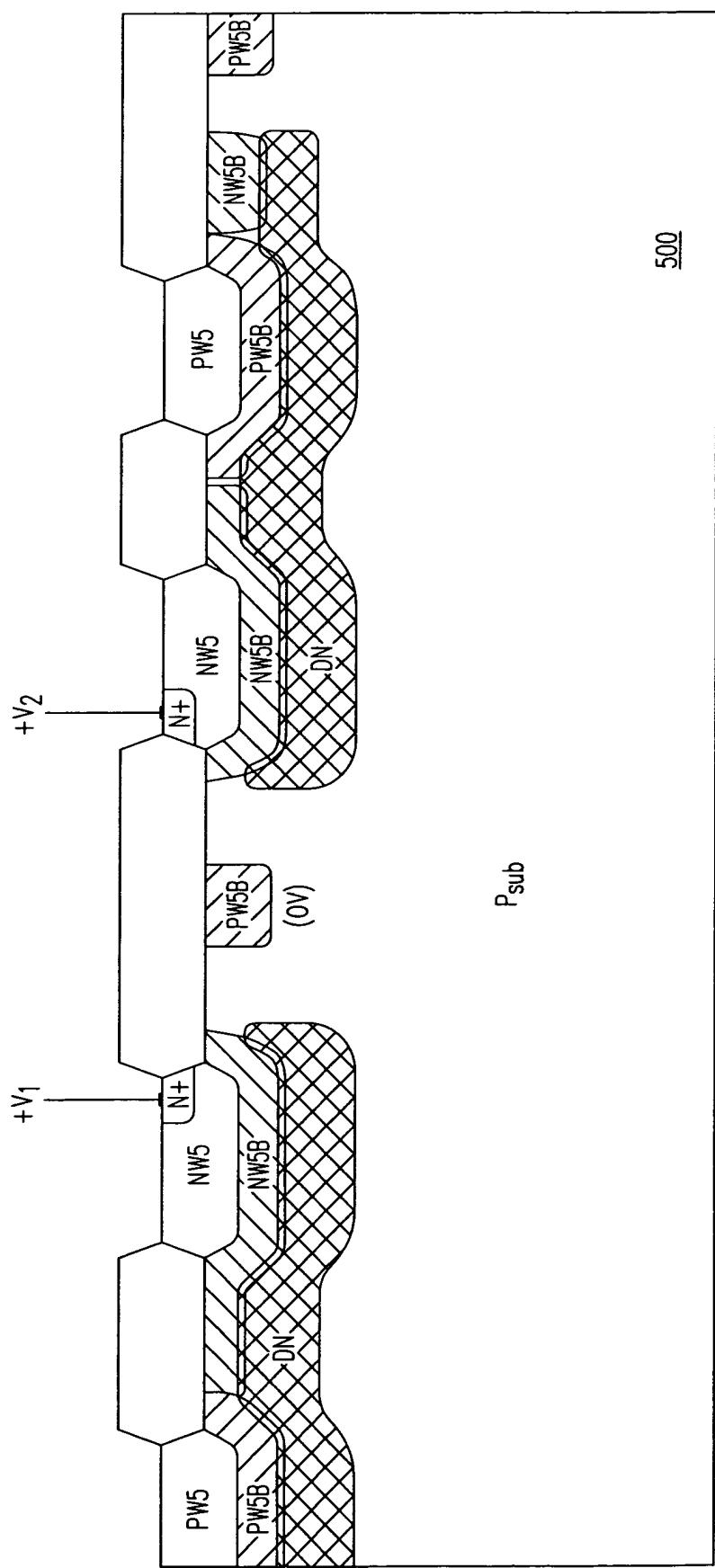


FIG. 16A

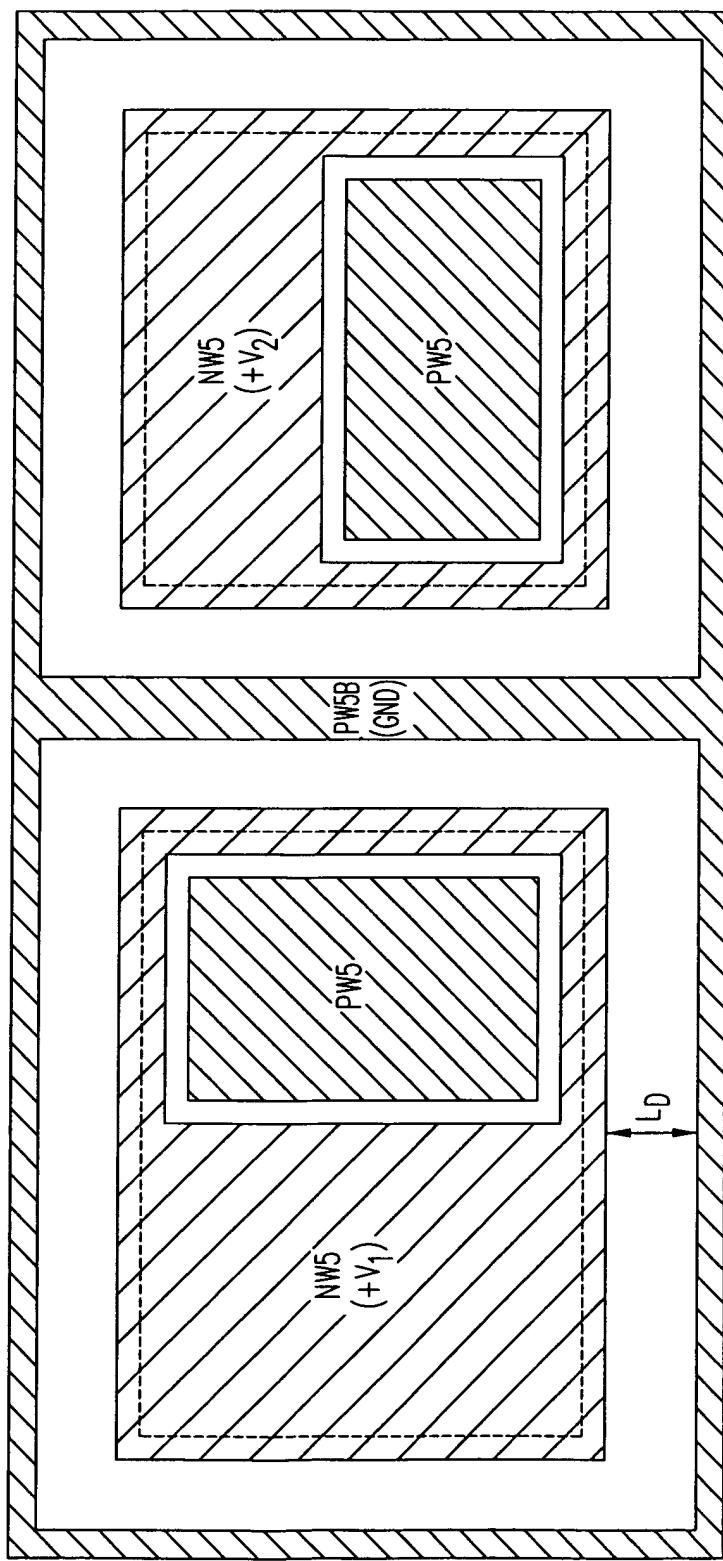
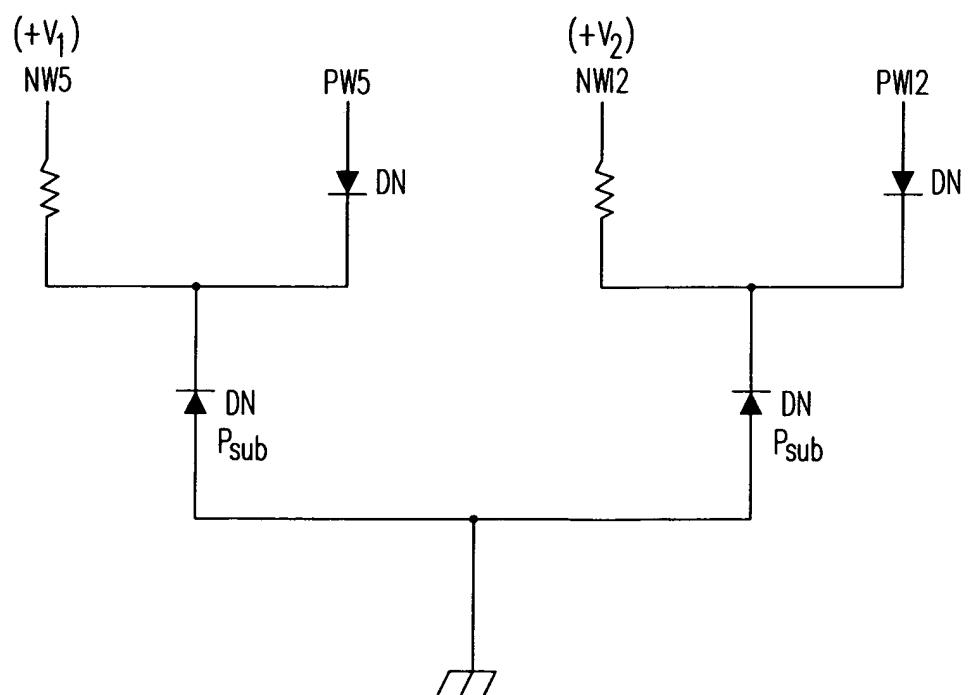
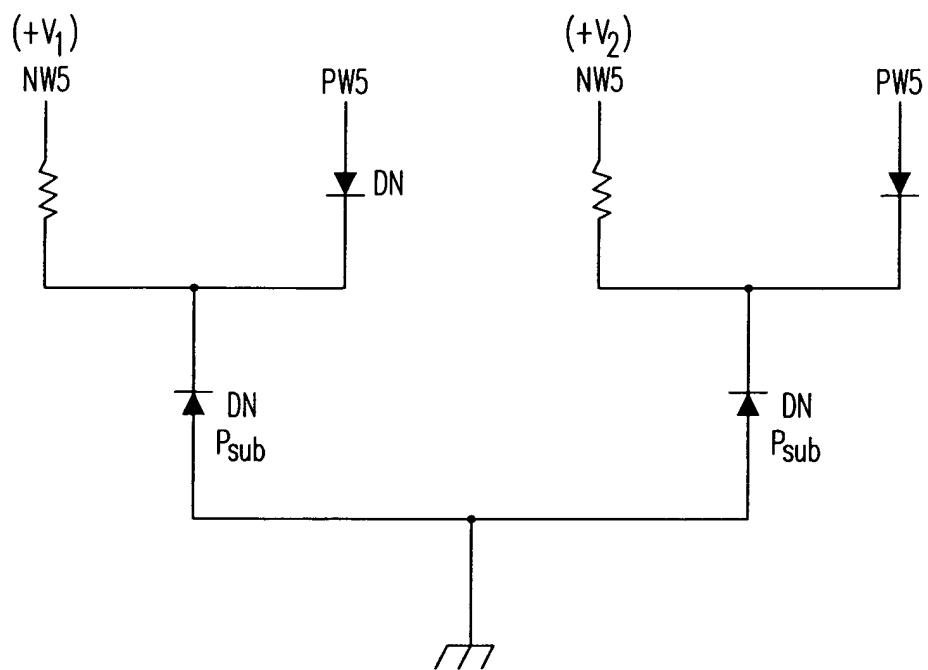


FIG. 16B



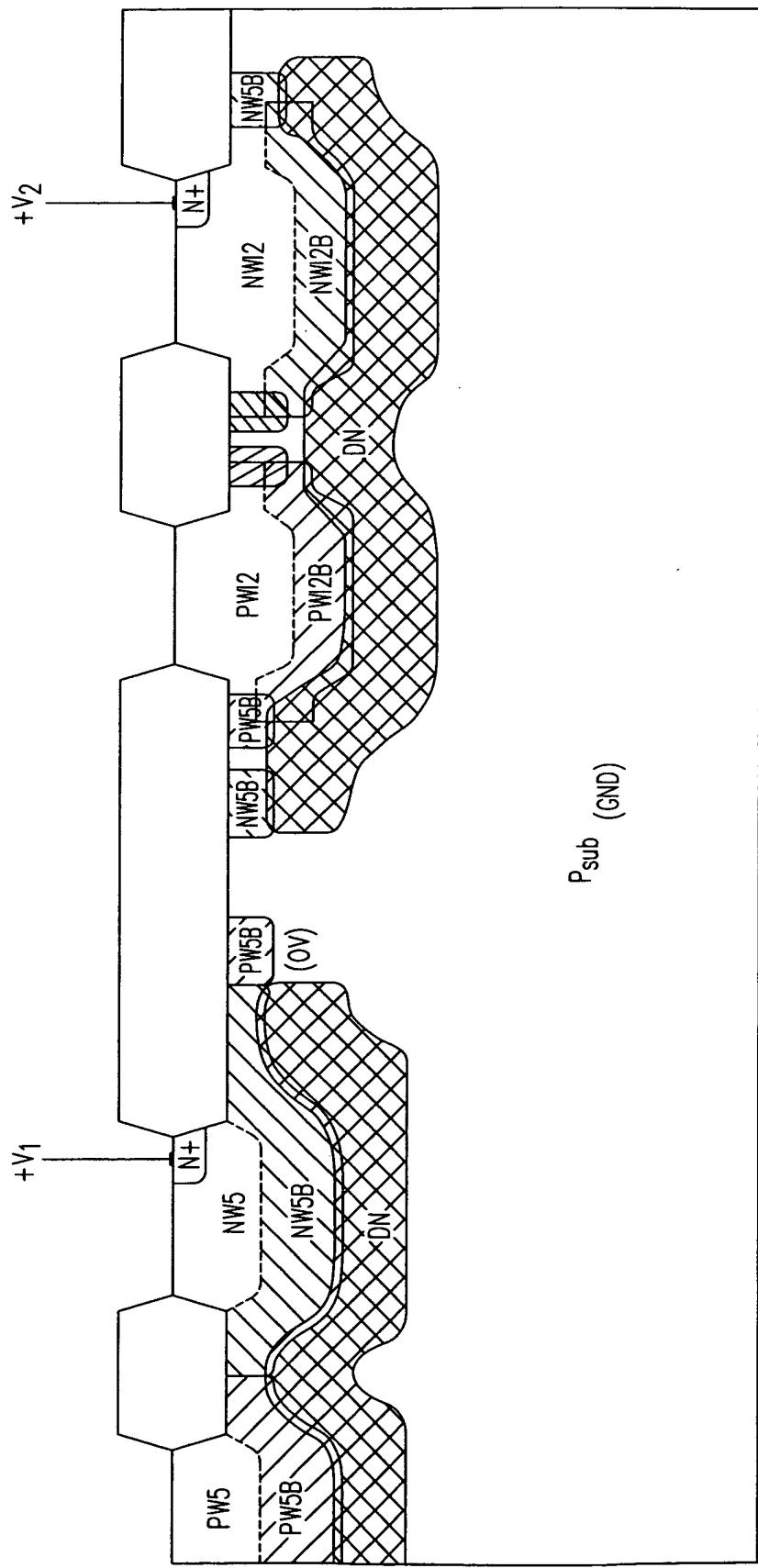


FIG. 16D

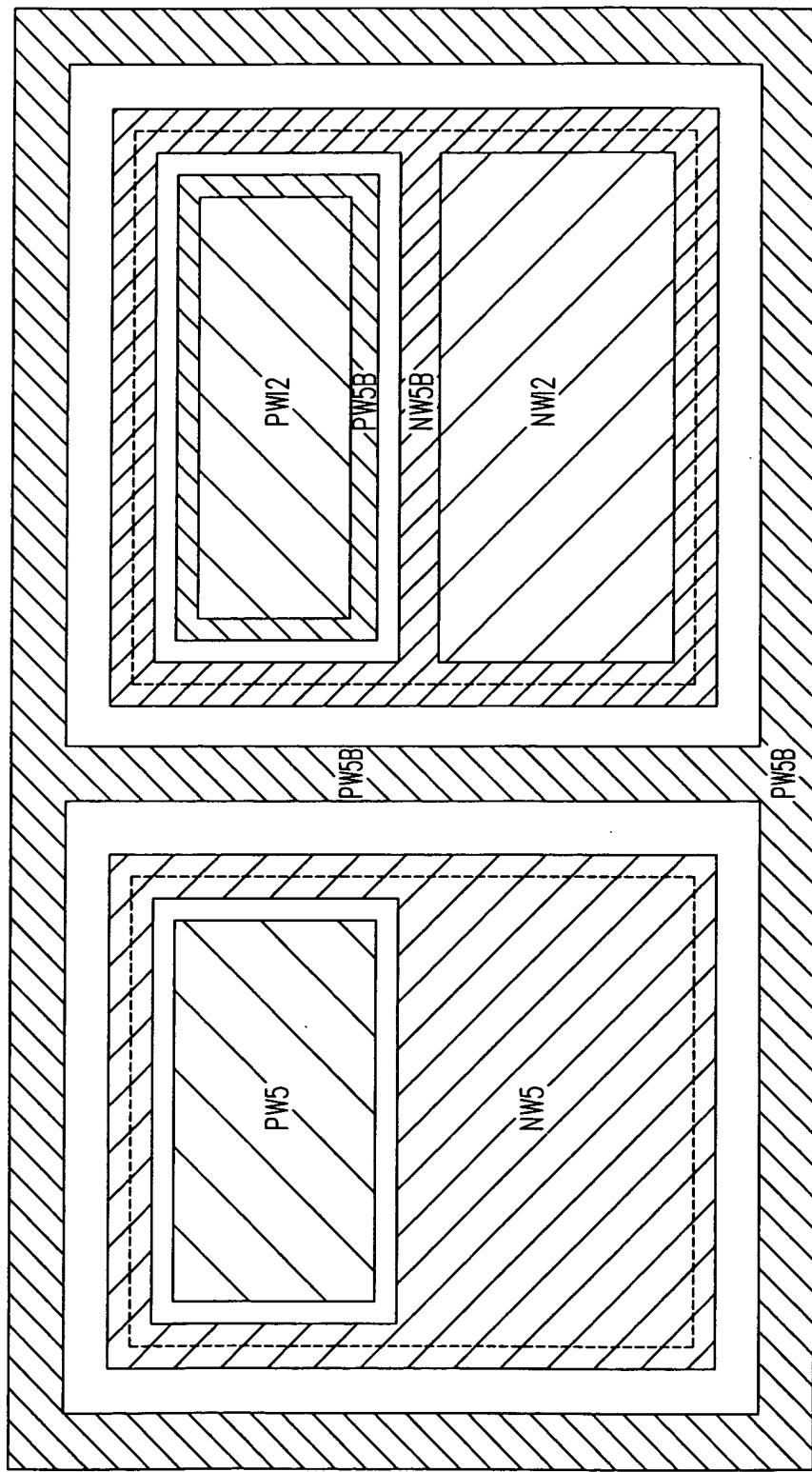


FIG. 16F

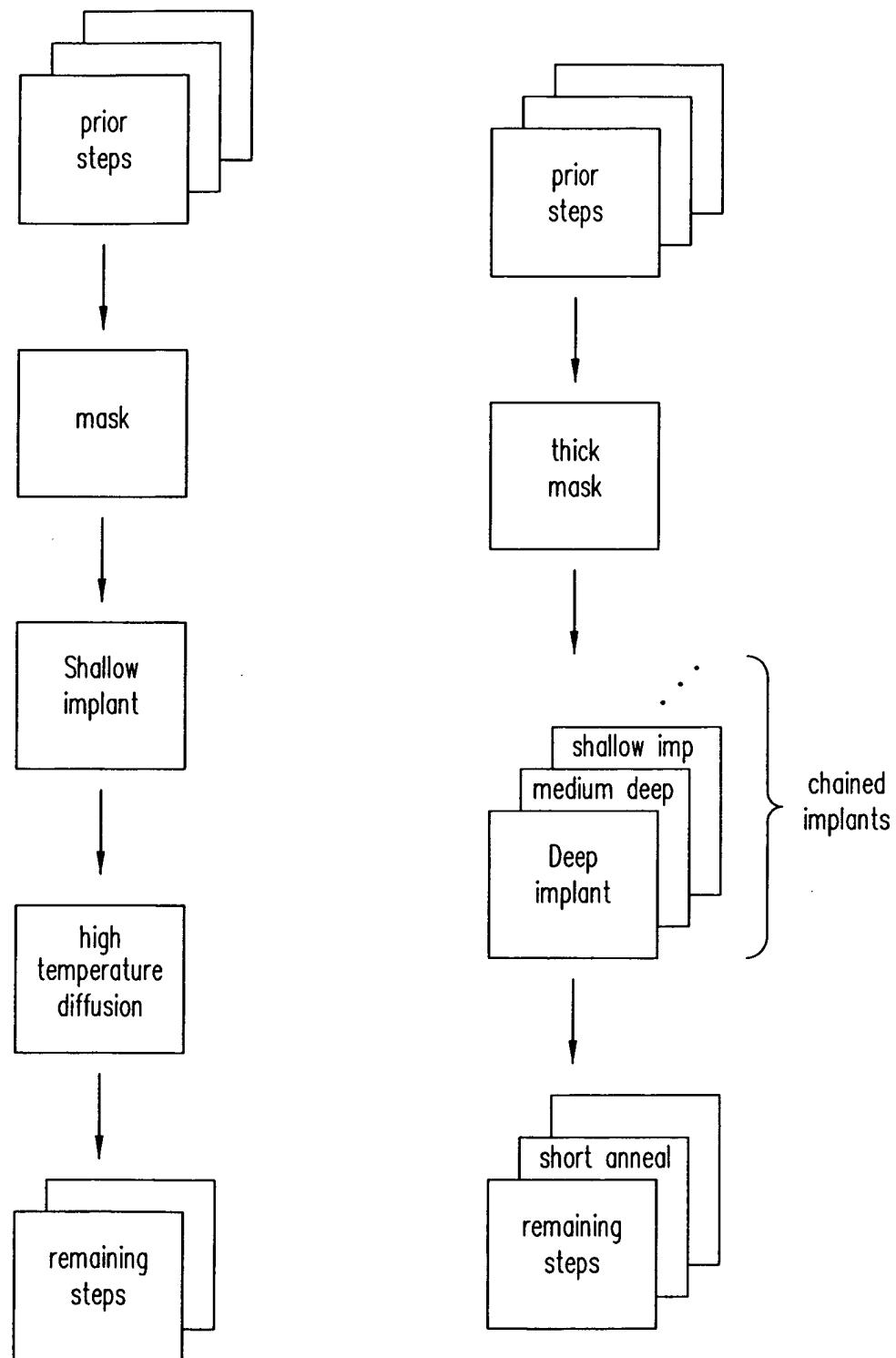


FIG. 17A
(Prior Art)

FIG. 17B

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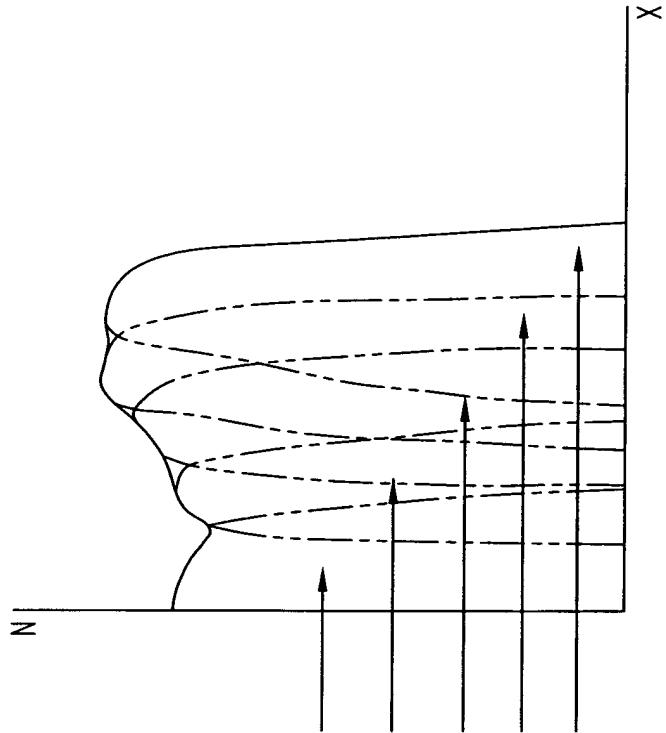


FIG. 17D

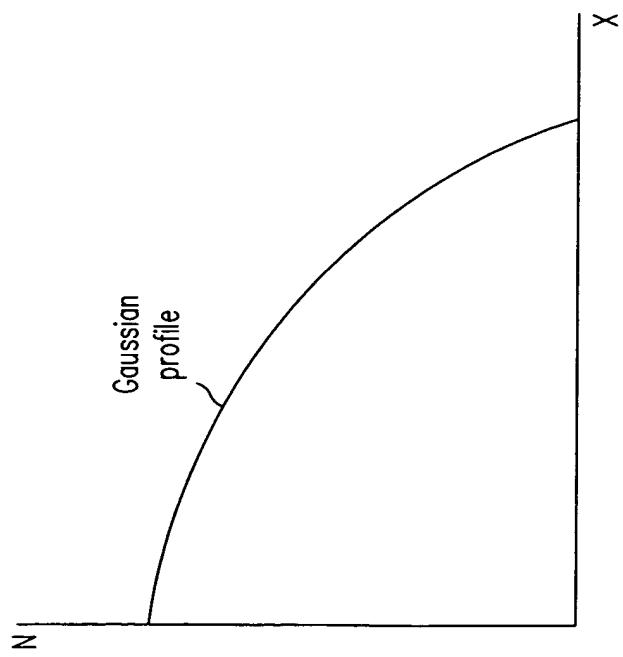


FIG. 17C
(Prior Art)

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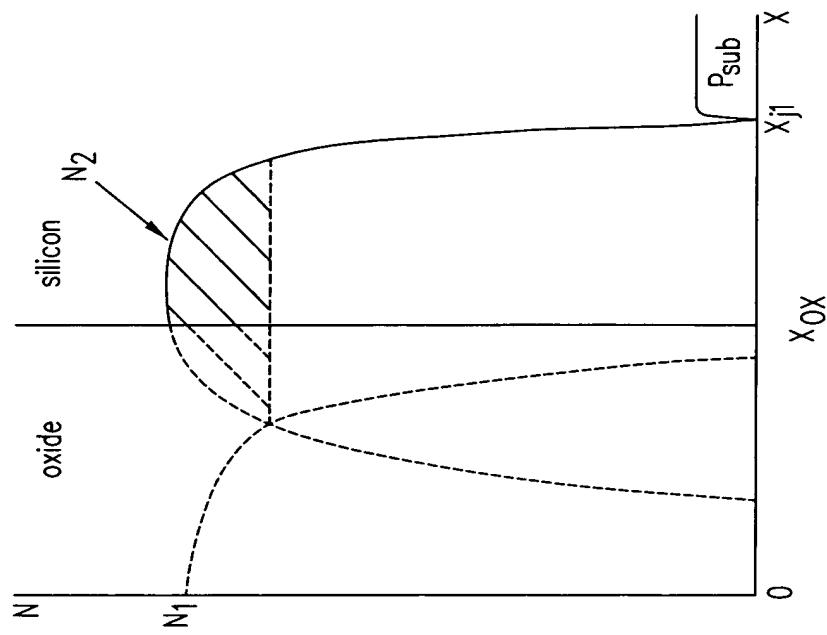


FIG. 17F

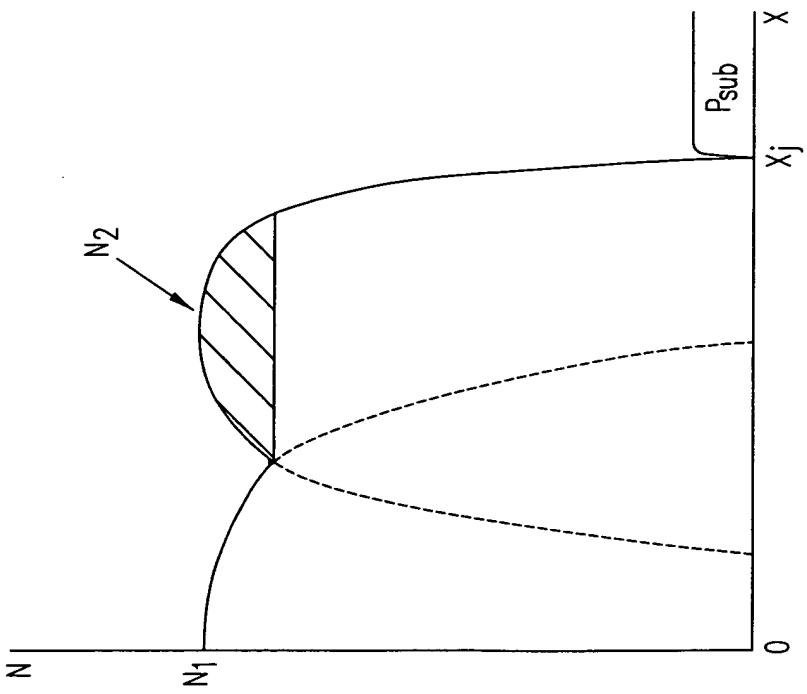


FIG. 17E

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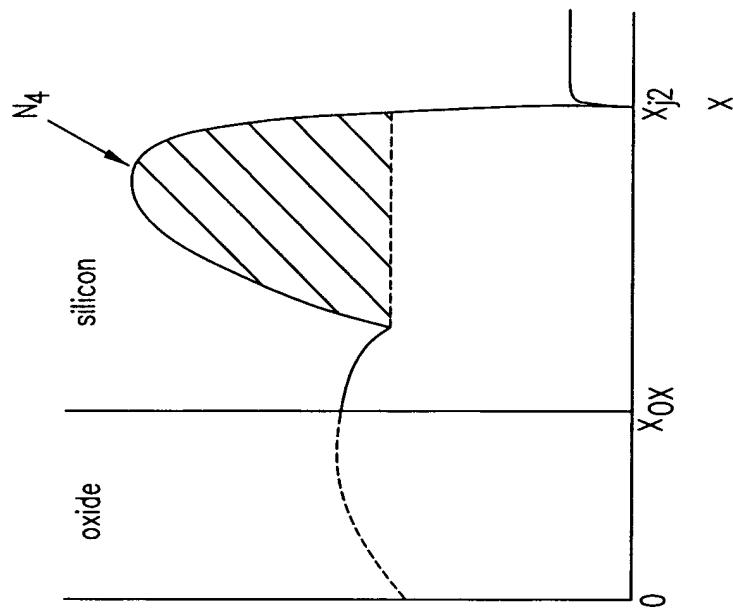


FIG. 17H

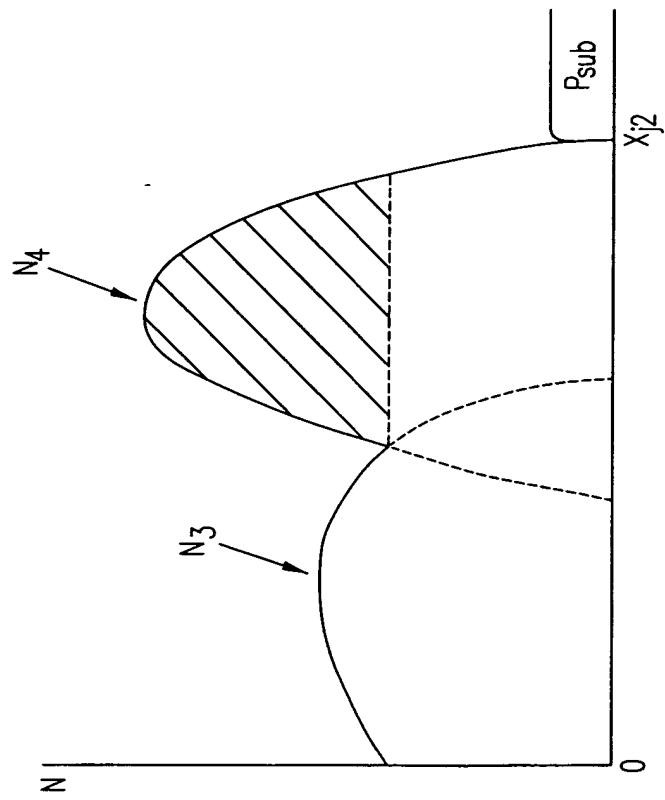


FIG. 17G

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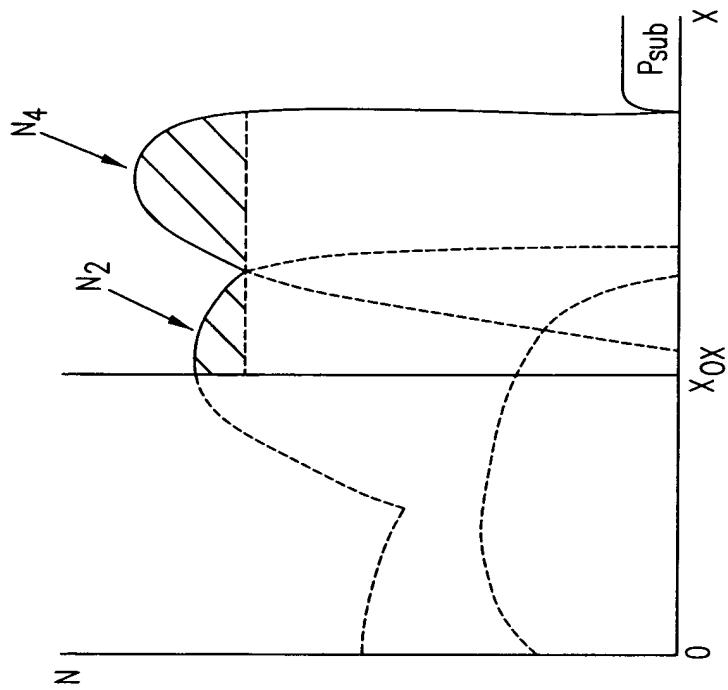


FIG. 17J

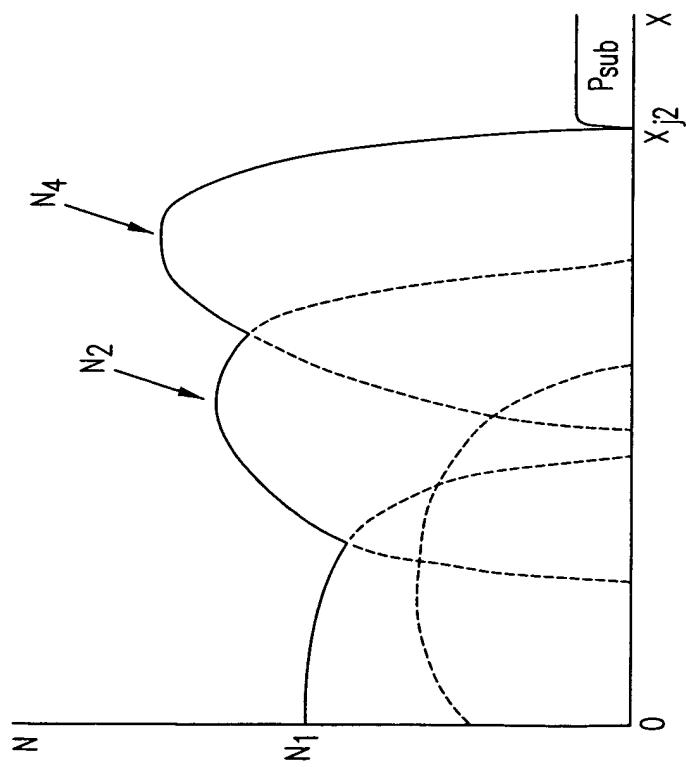


FIG. 17I

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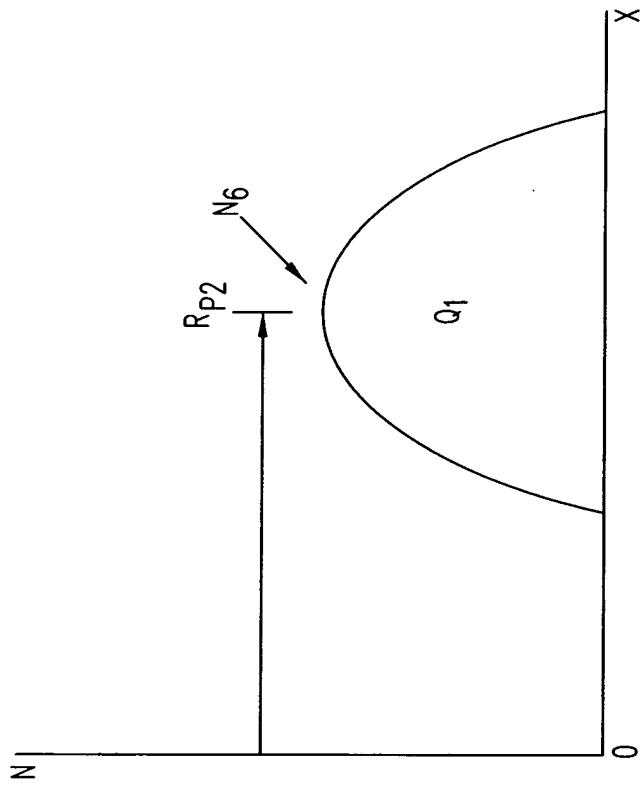


FIG. 17L
(Prior Art)

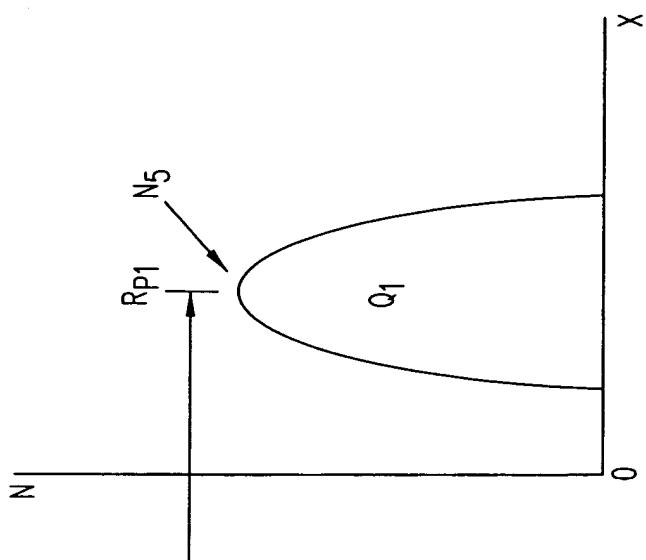


FIG. 17K
(Prior Art)

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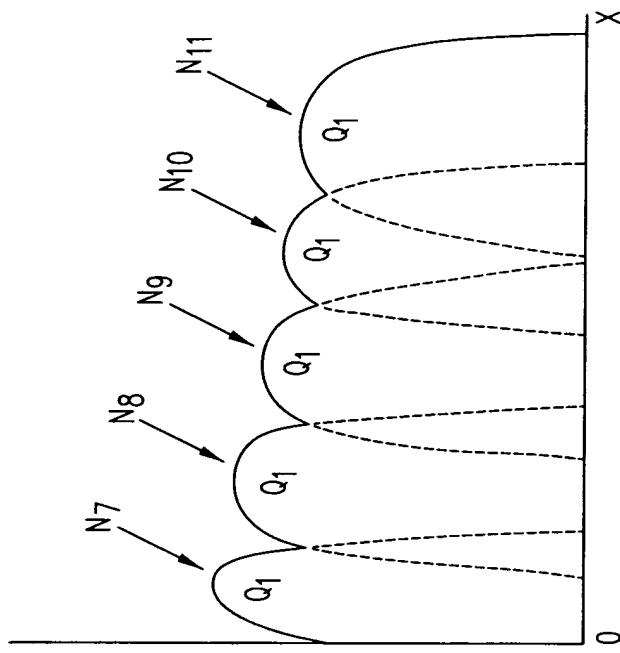


FIG. 17N

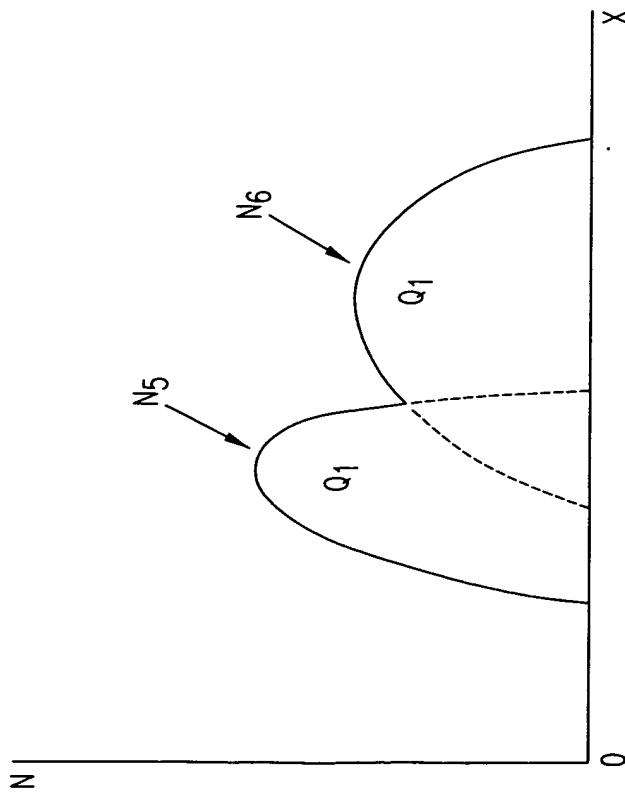


FIG. 17M

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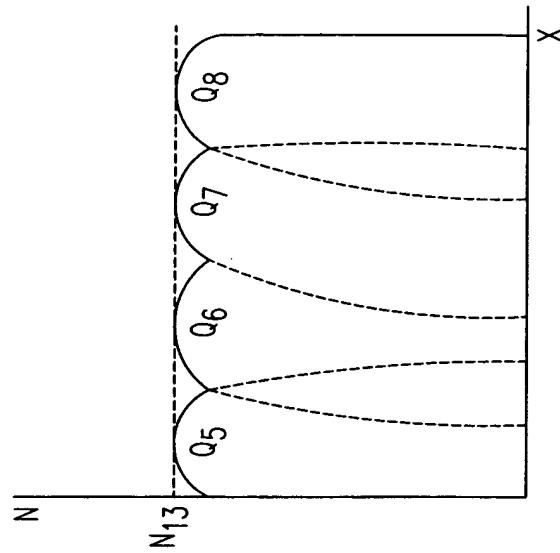


FIG. 17Q

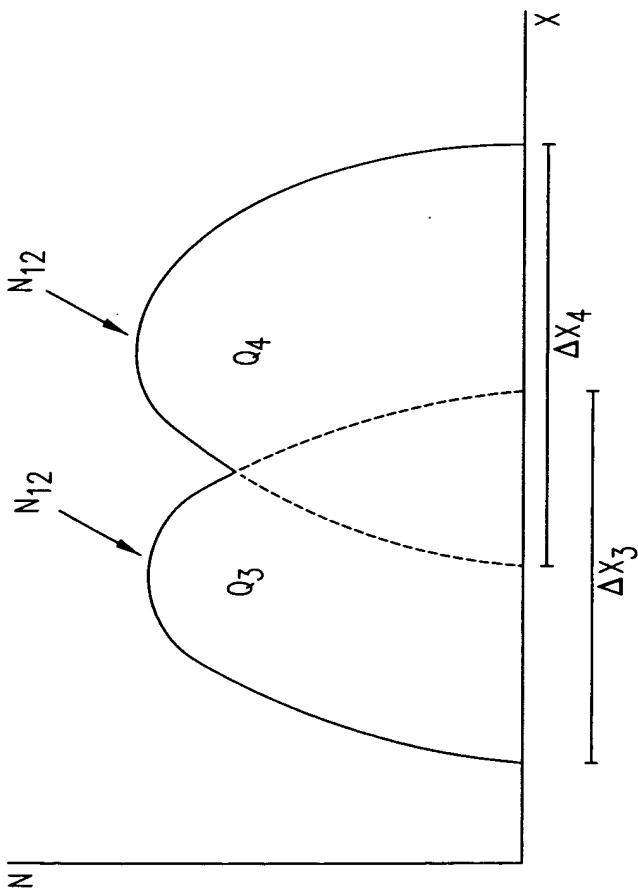


FIG. 17P

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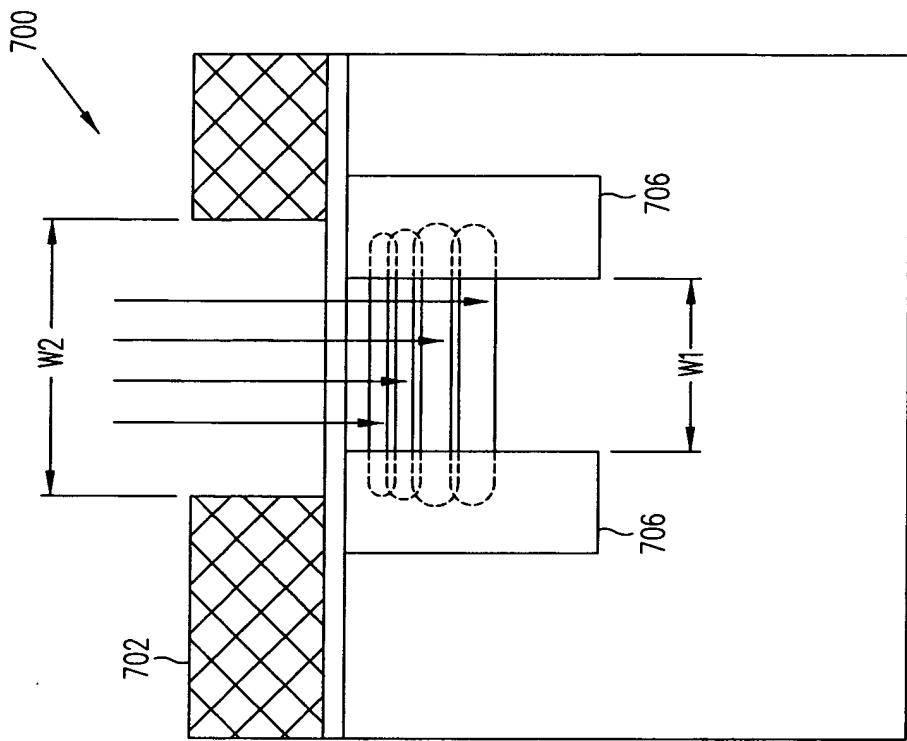


FIG. 17S

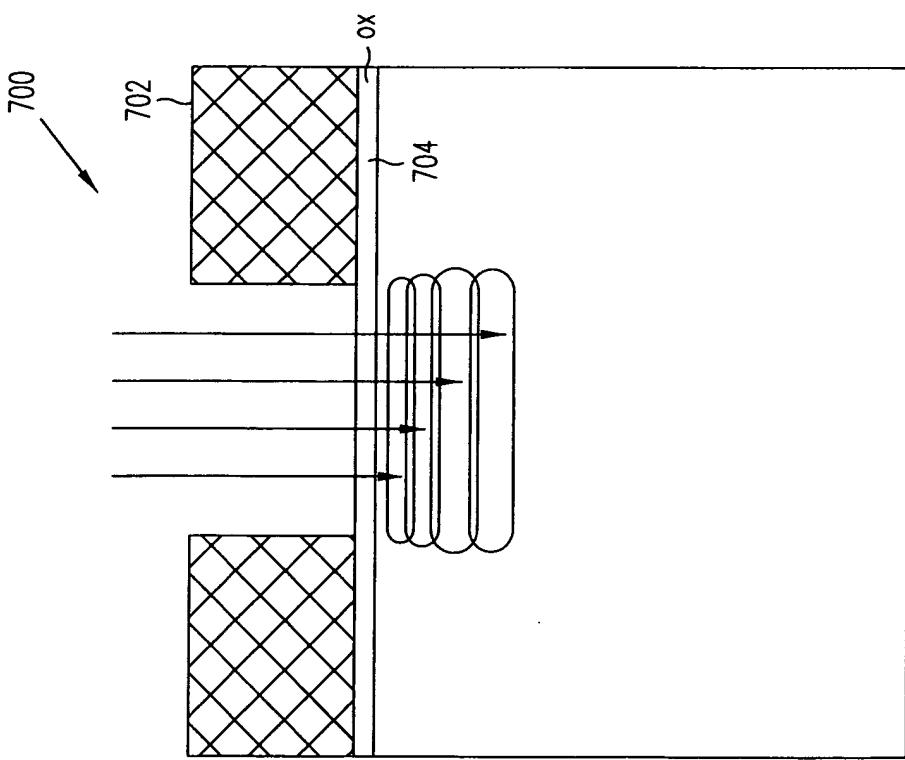


FIG. 17R

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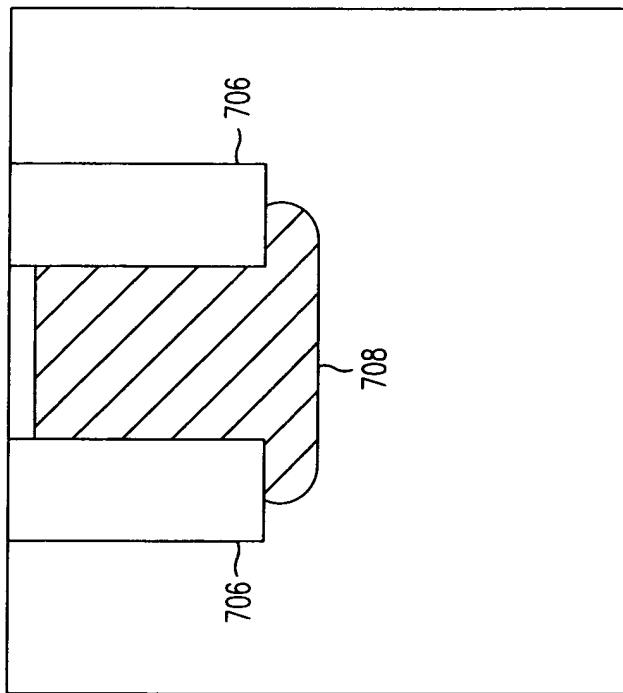


FIG. 17U

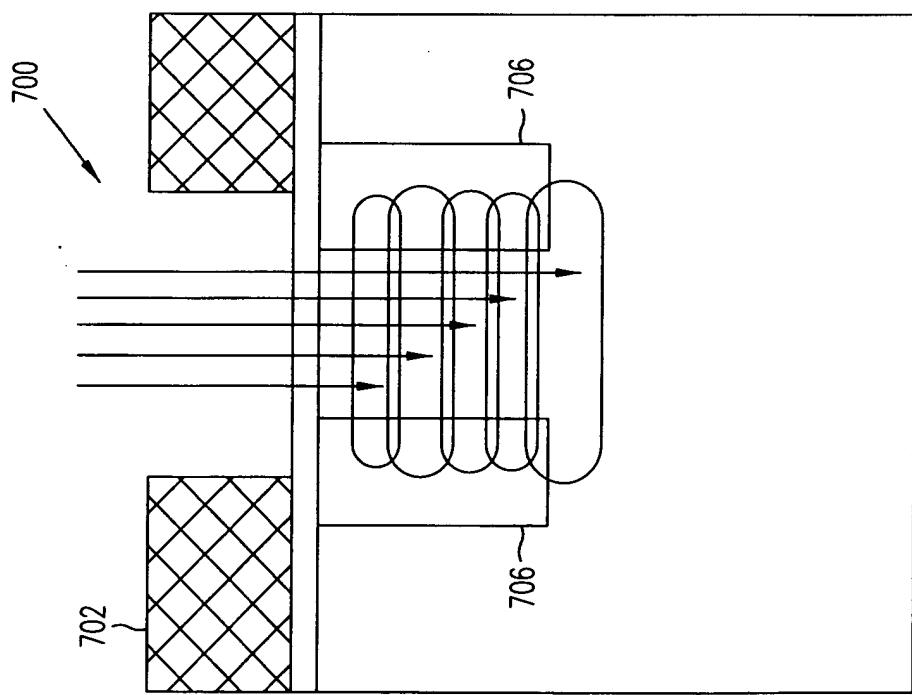


FIG. 17T

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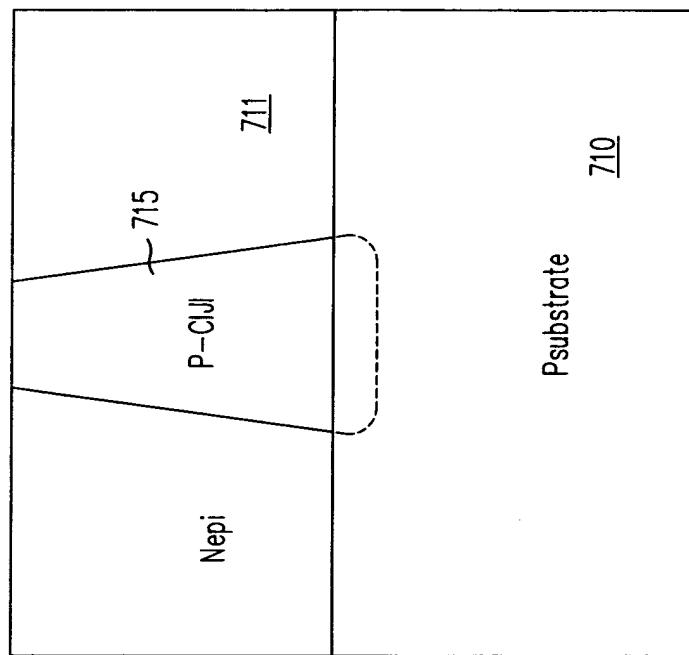


FIG. 17V

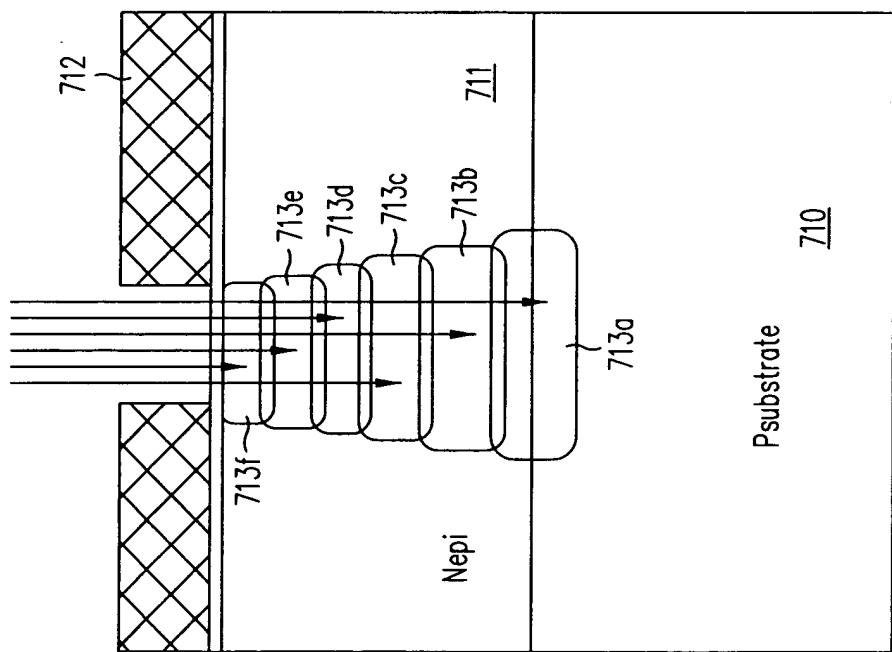


FIG. 17U

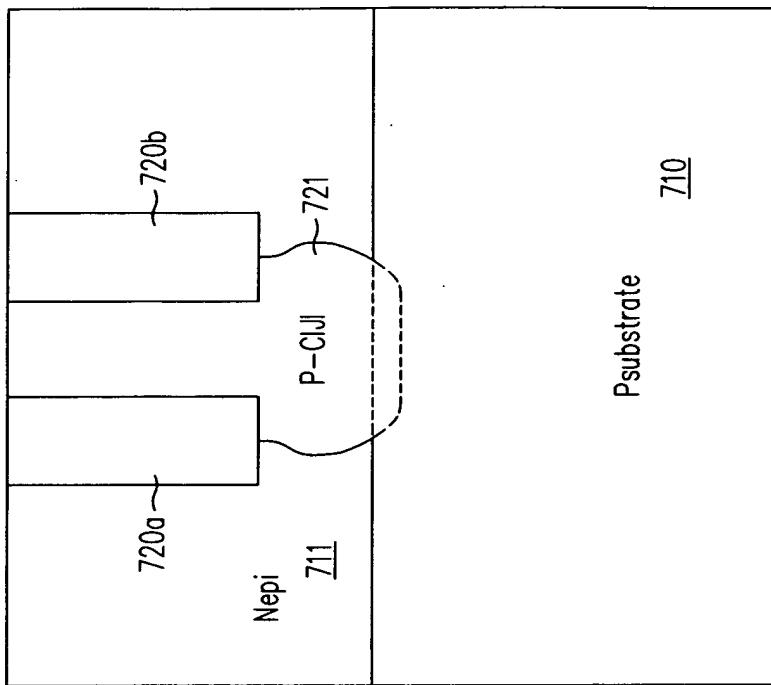


FIG. 17X

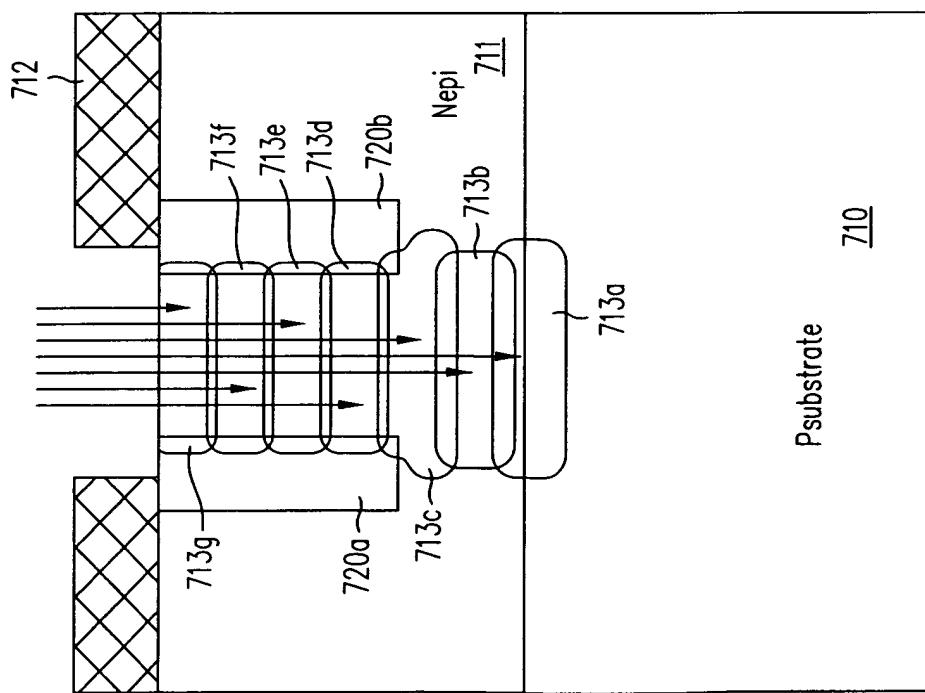


FIG. 17W

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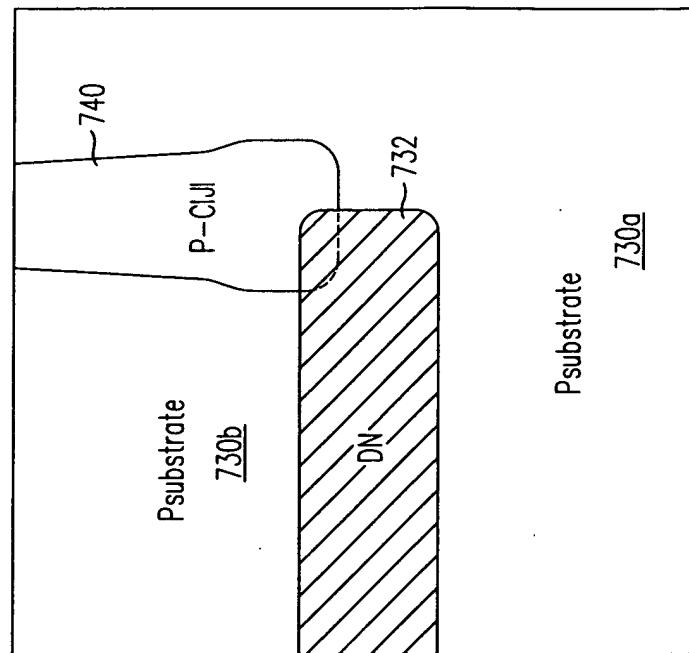


FIG. 17Z

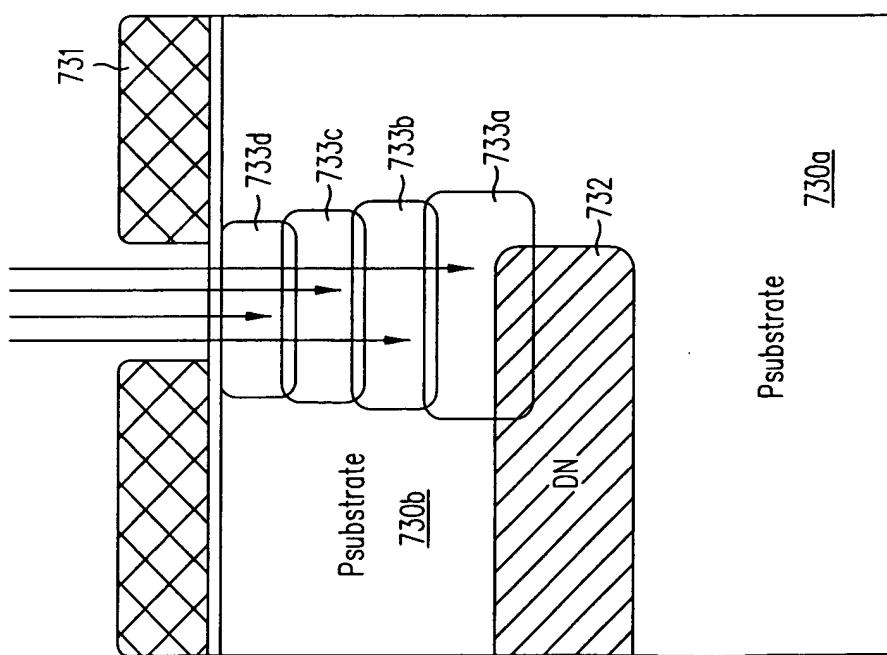


FIG. 17Y

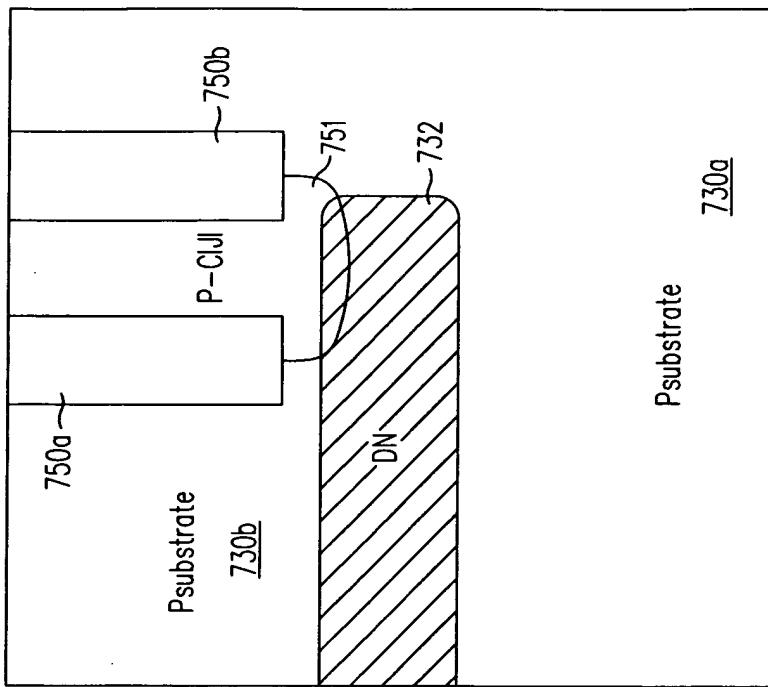


FIG. 17BB

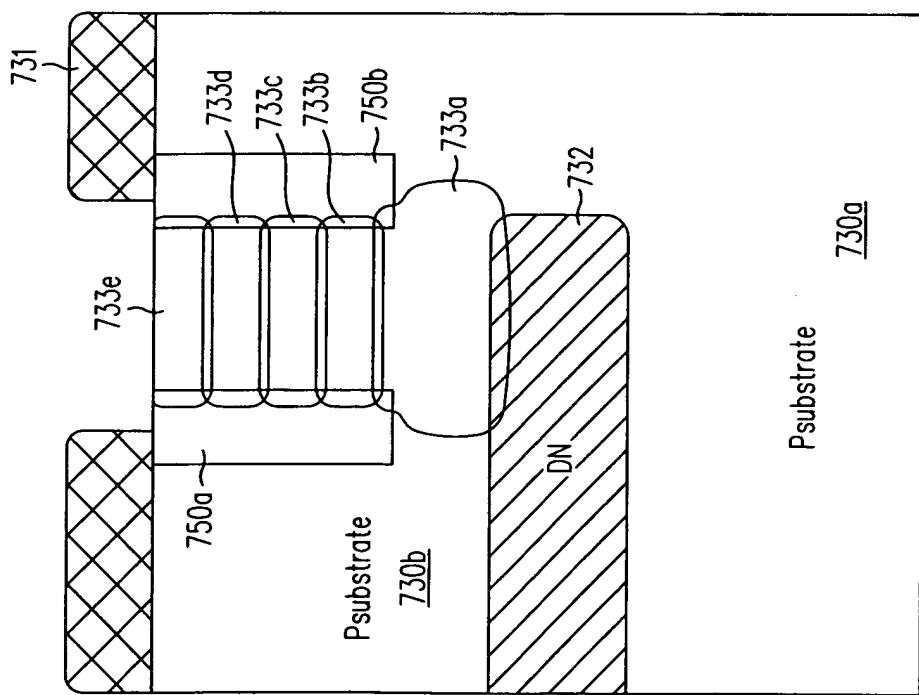


FIG. 17AA

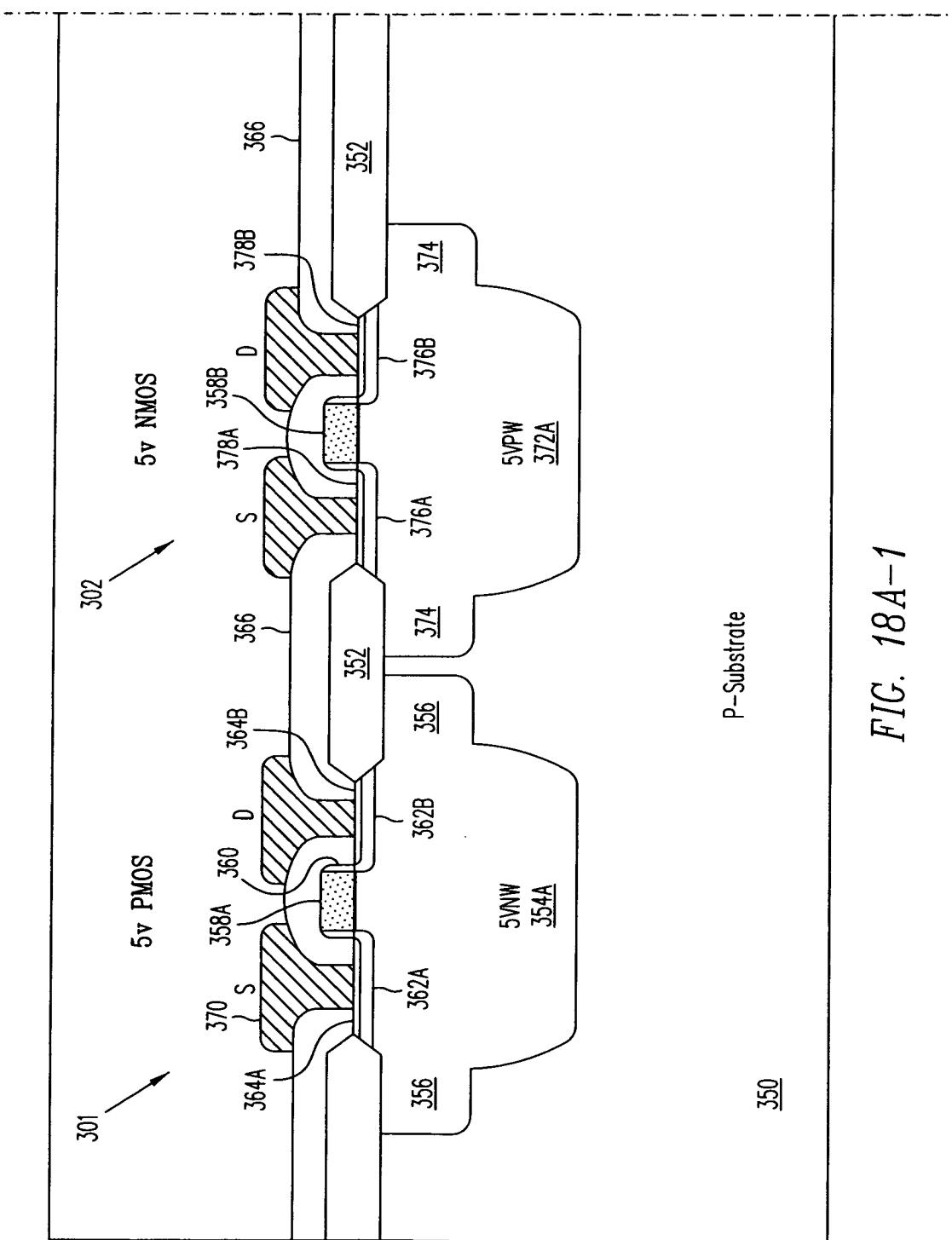


FIG. 18A-1

P-Substrate

350

Key To
FIG. 18A

FIG. 18A-1	FIG. 18A-2
FIG. 18A-3	FIG. 18A-4

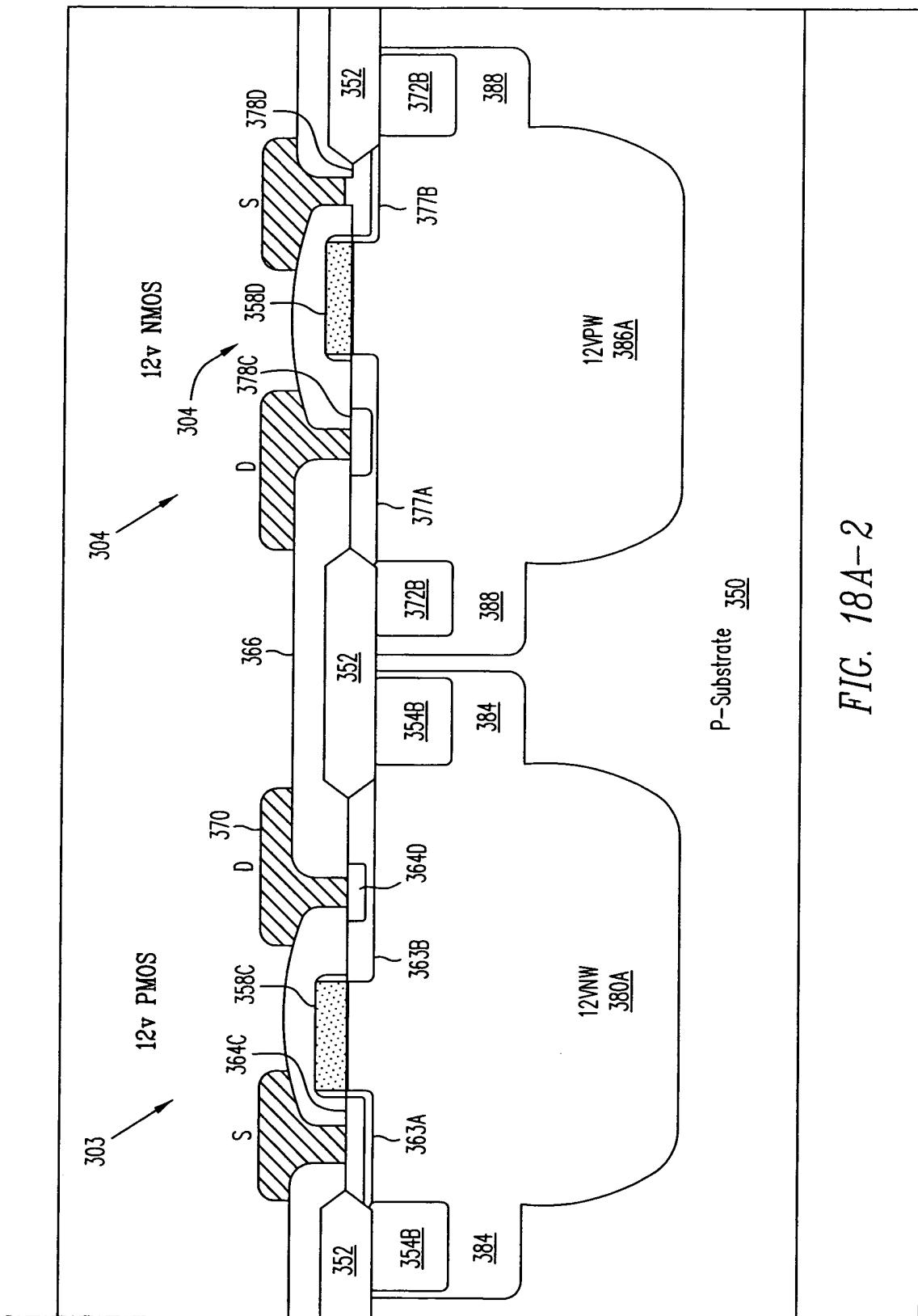


FIG. 18A-2

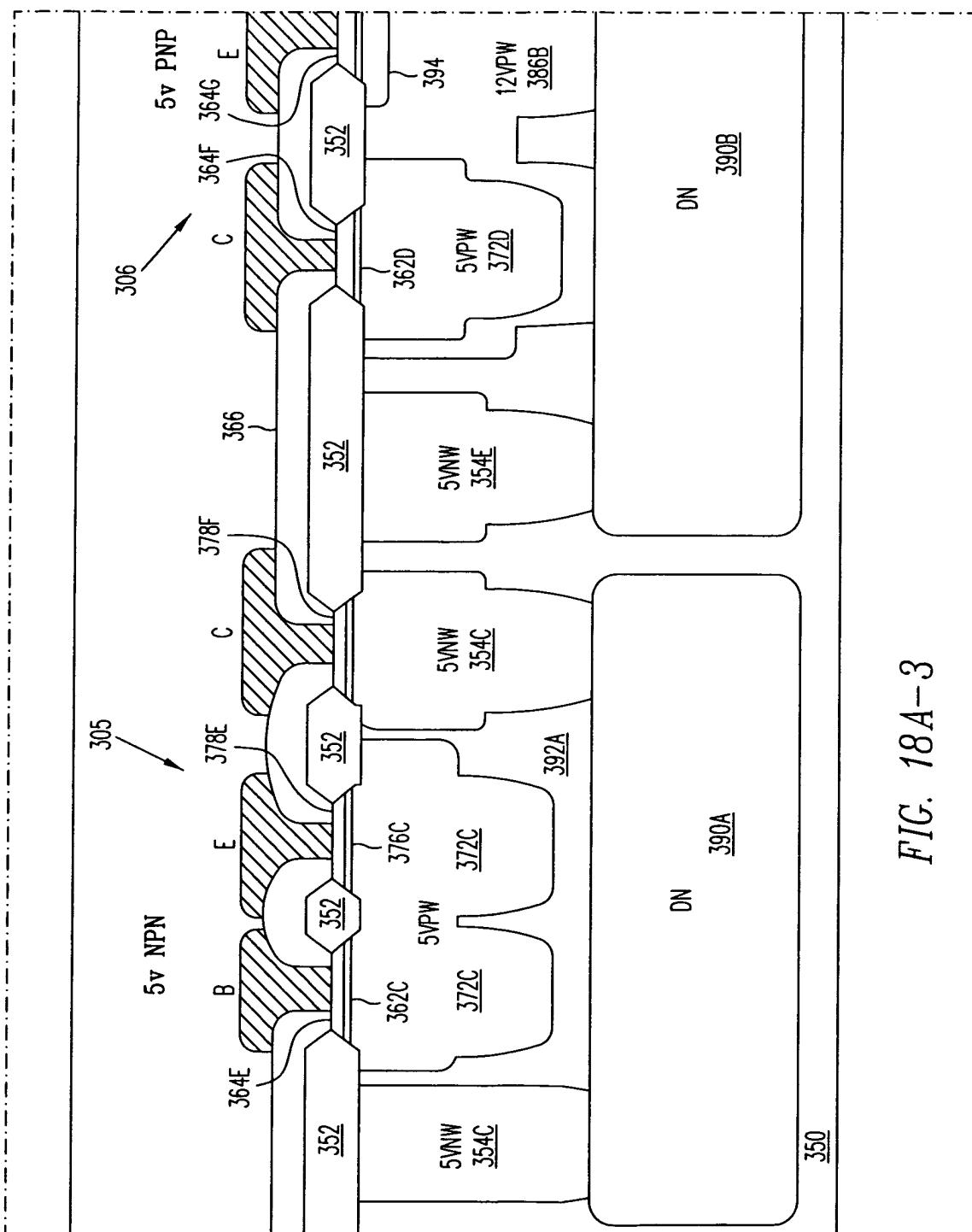


FIG. 18A-3

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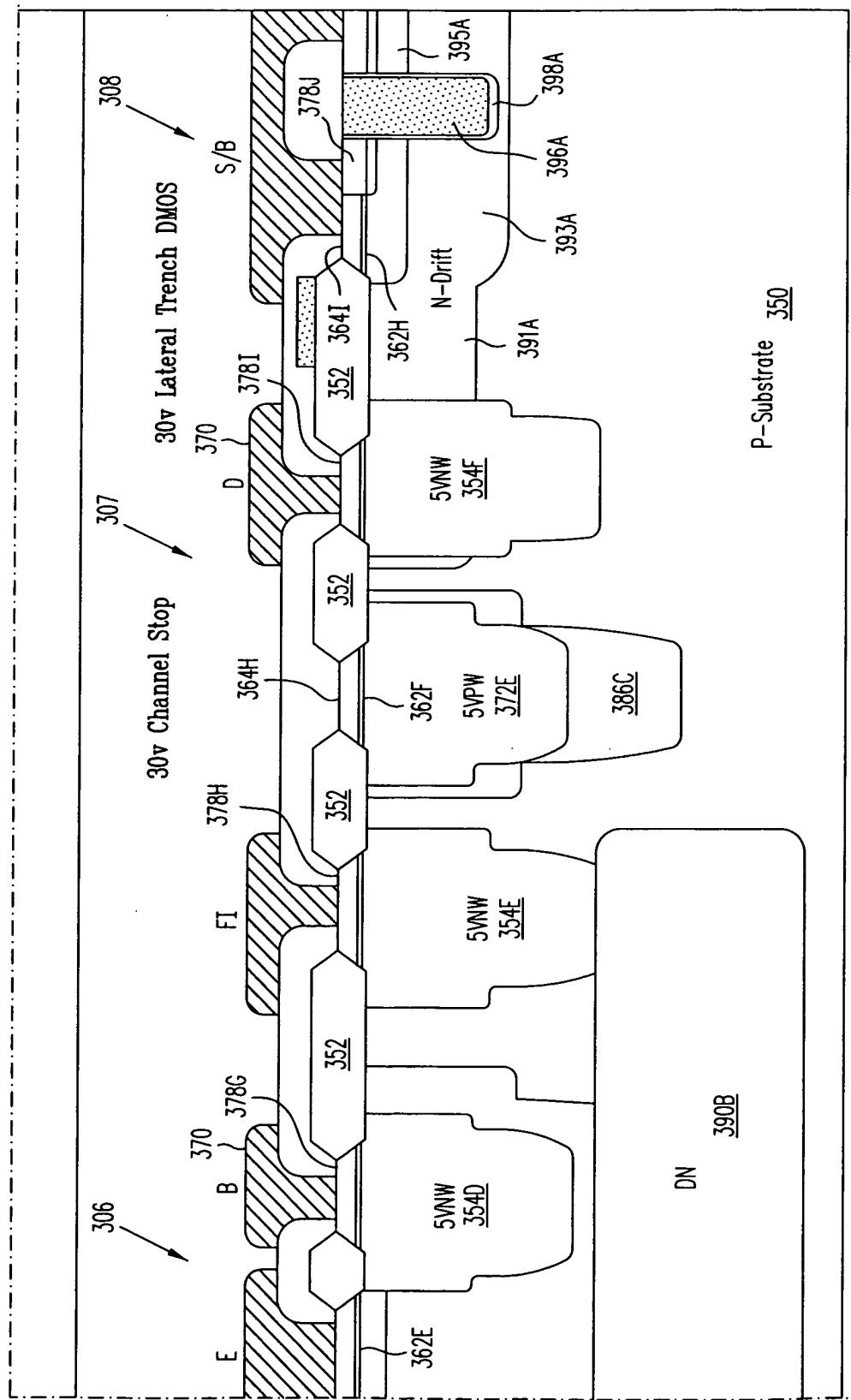


FIG. 18A-4

FIG. 18B-1

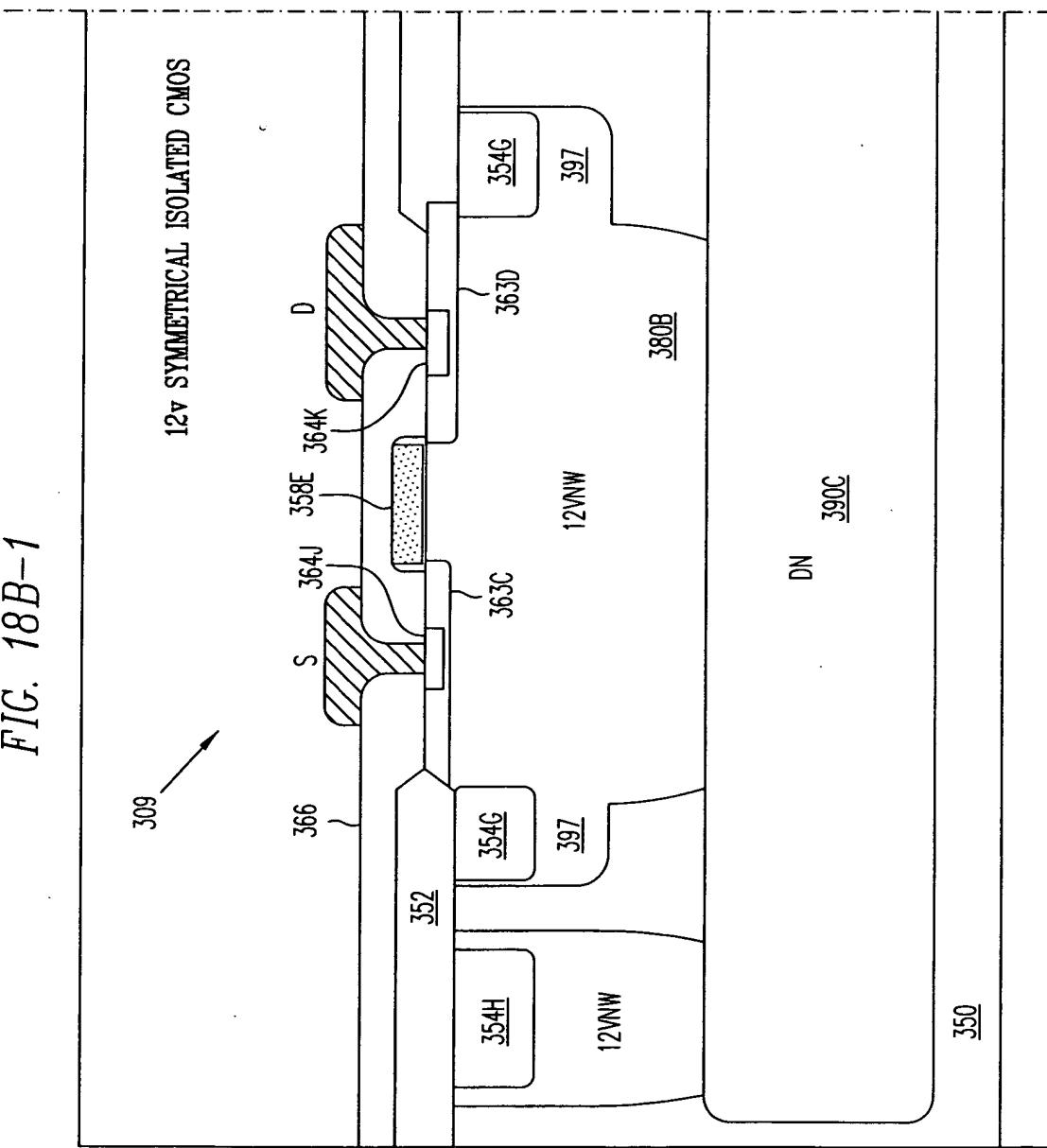
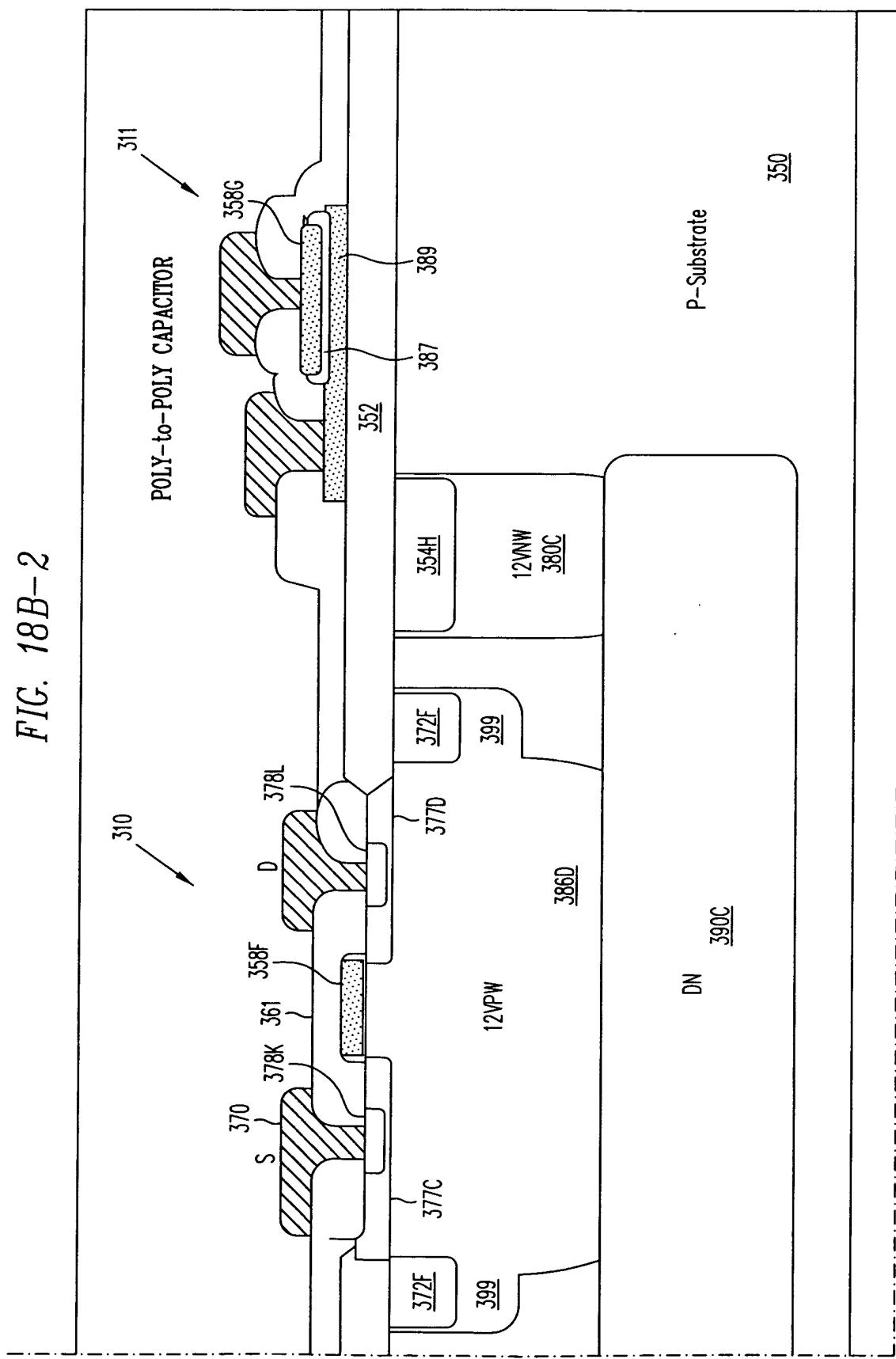


FIG. 18B-1	FIG. 18B-2
FIG. 18B-3	FIG. 18B-4

Key To
FIG. 18B

FIG. 18B-2



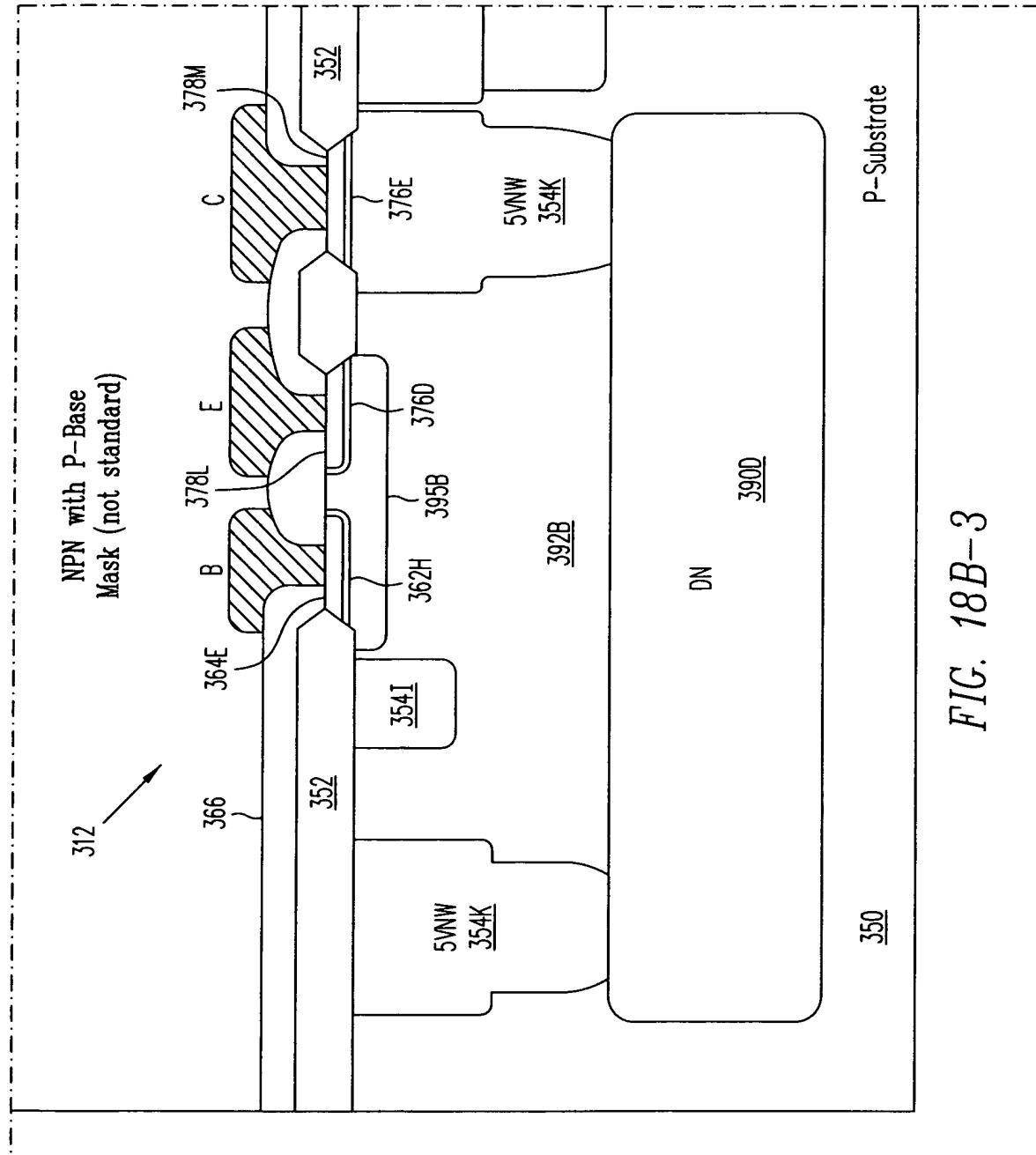


FIG. 18B-3

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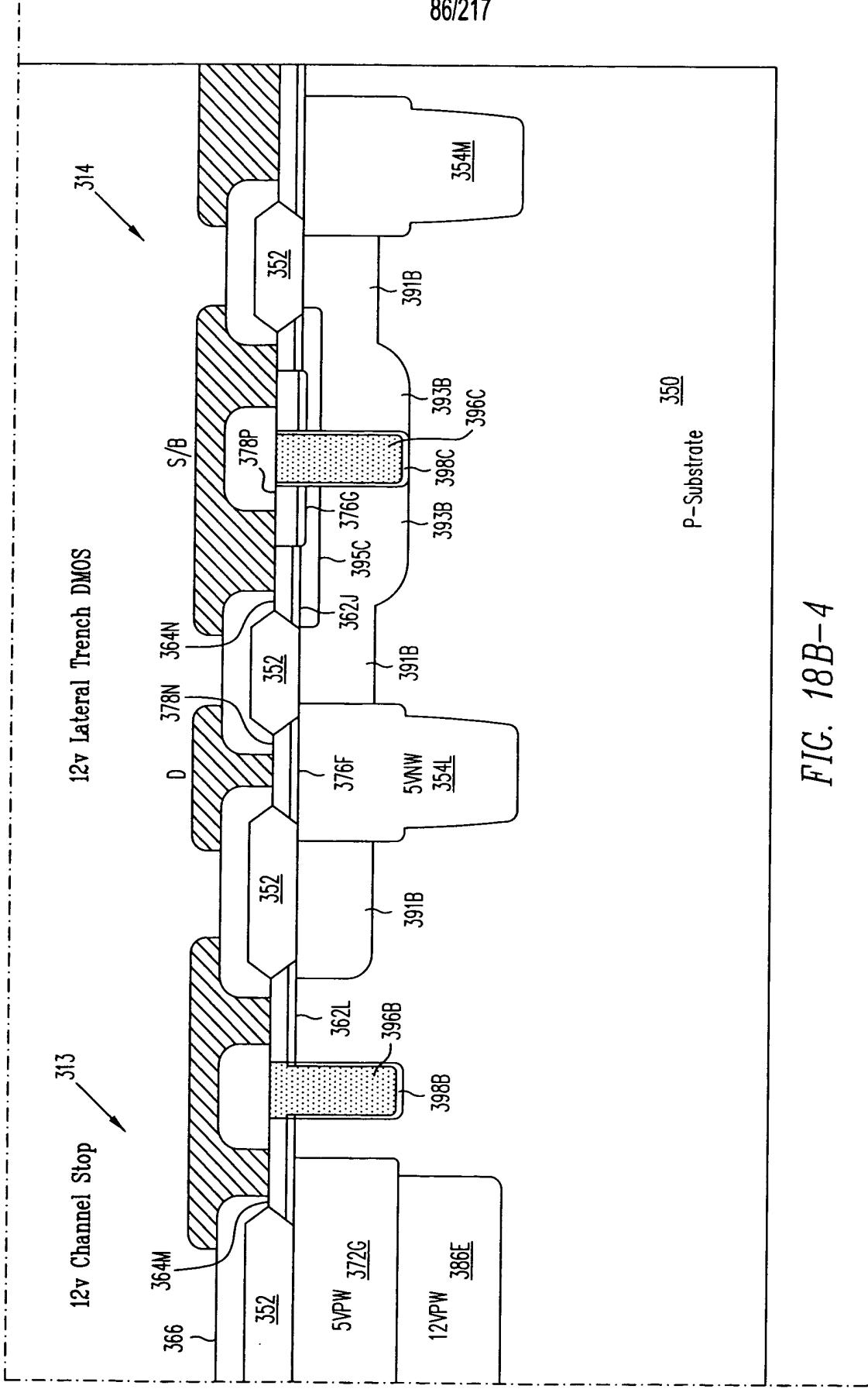


FIG. 18B-4

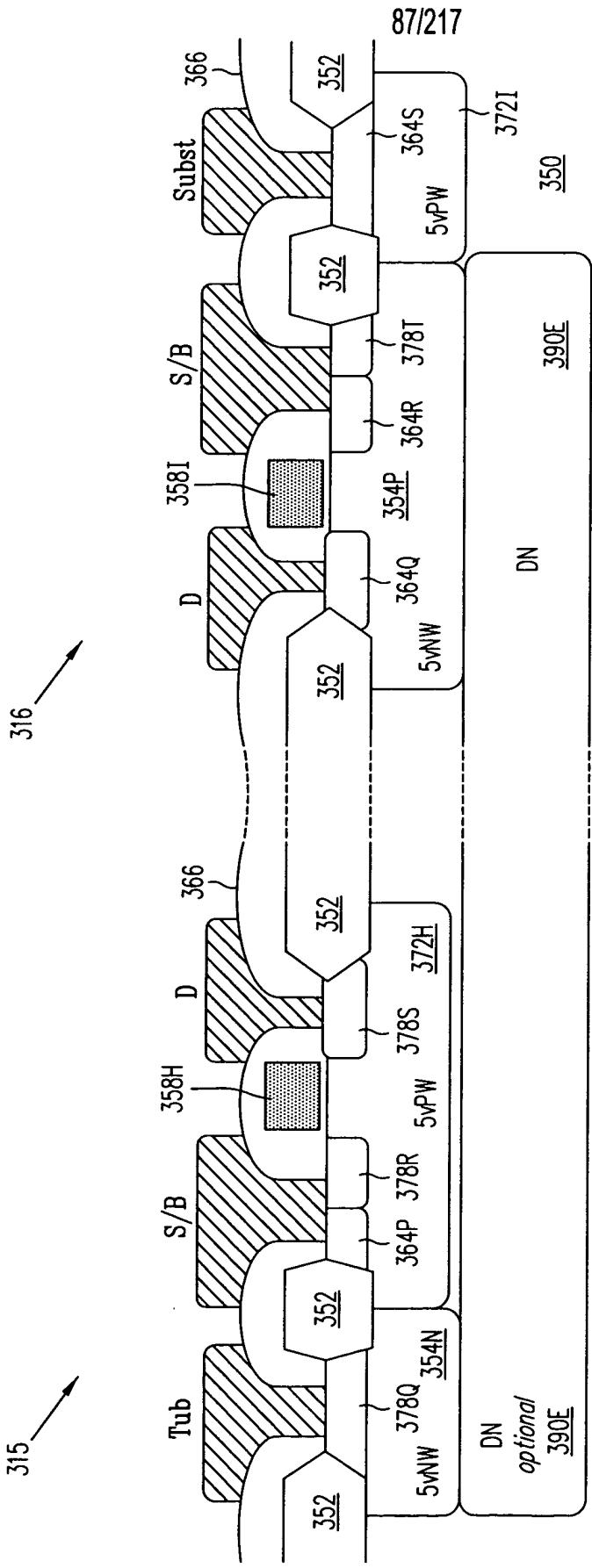


FIG. 18C

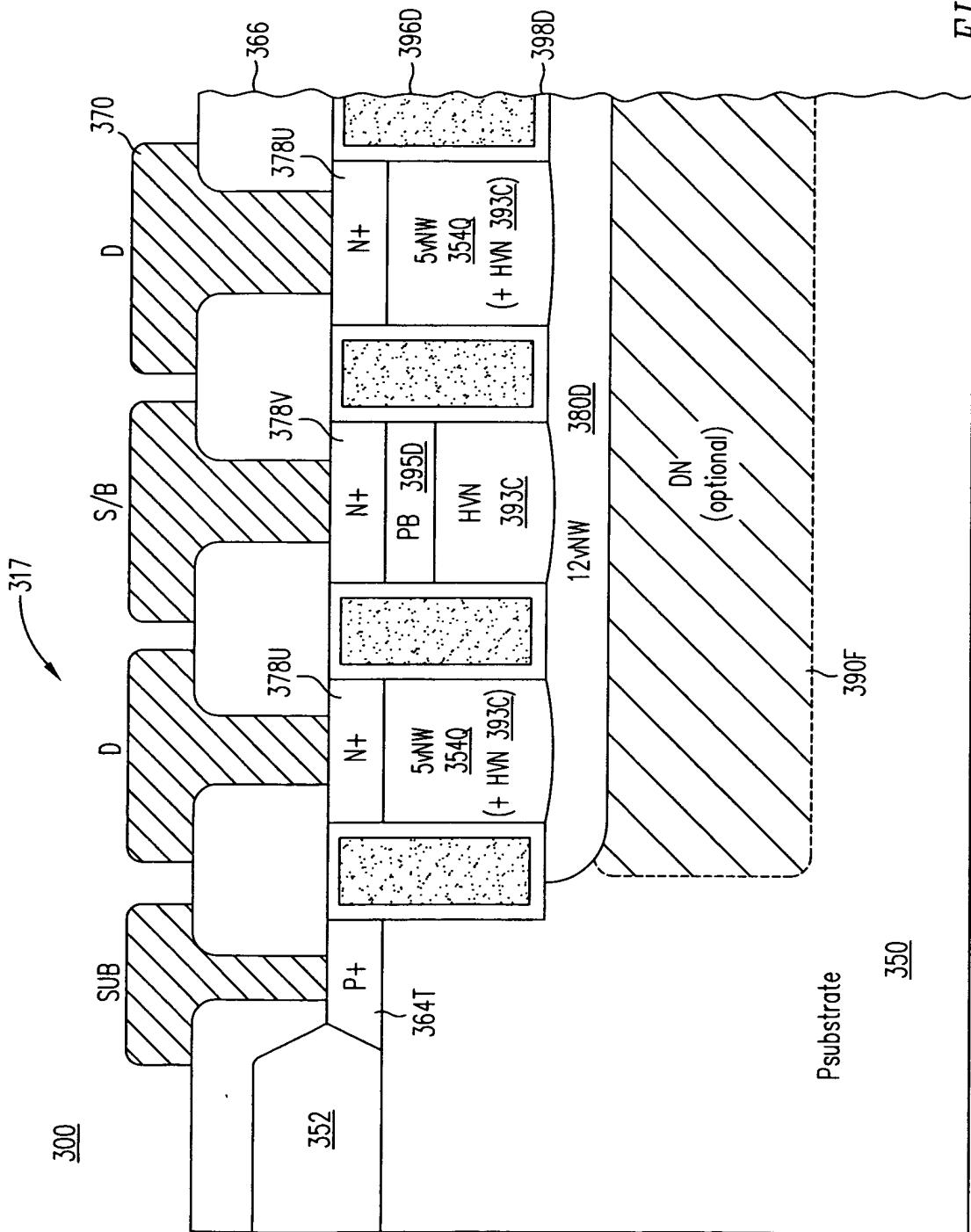


FIG. 18D

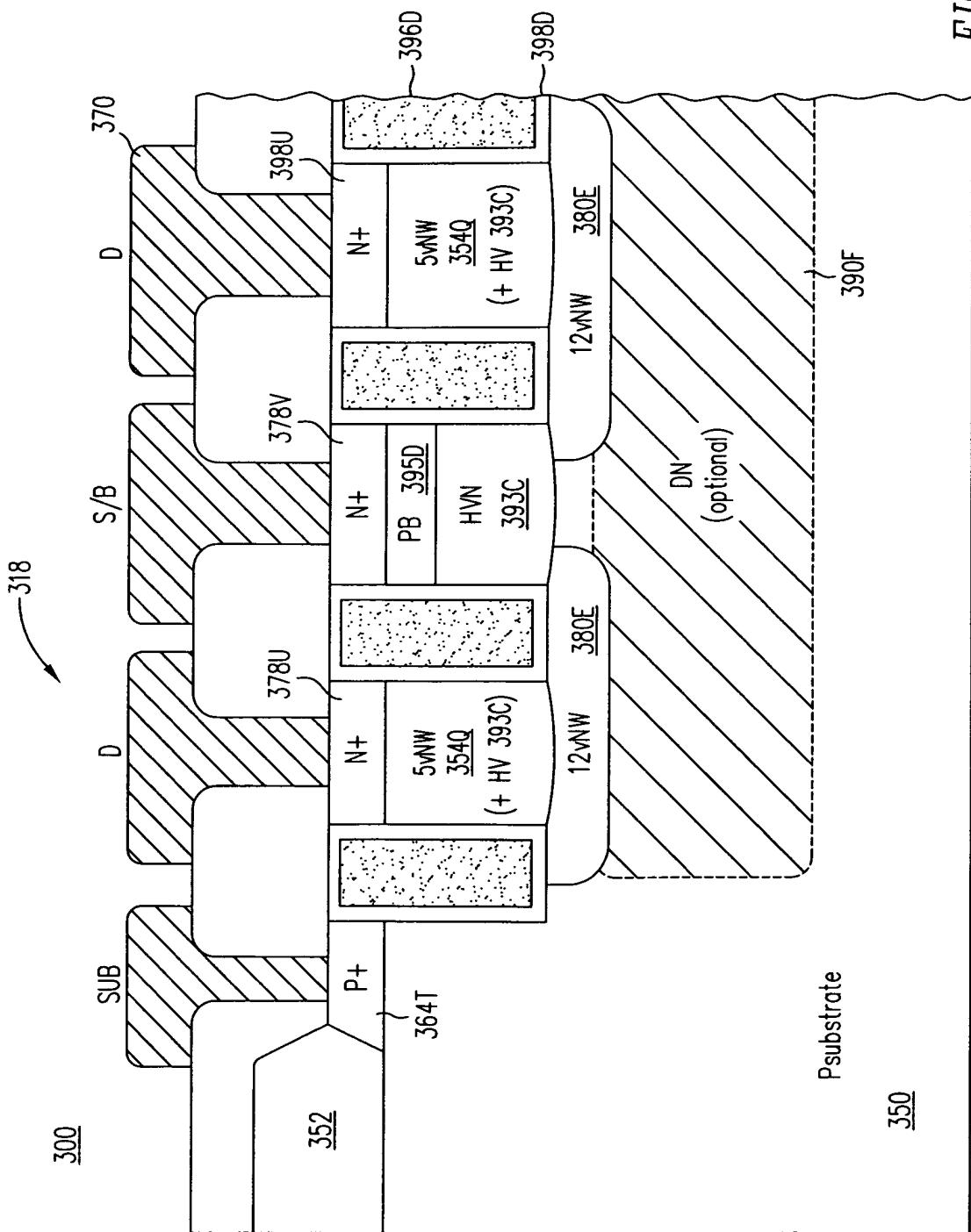


FIG. 18E

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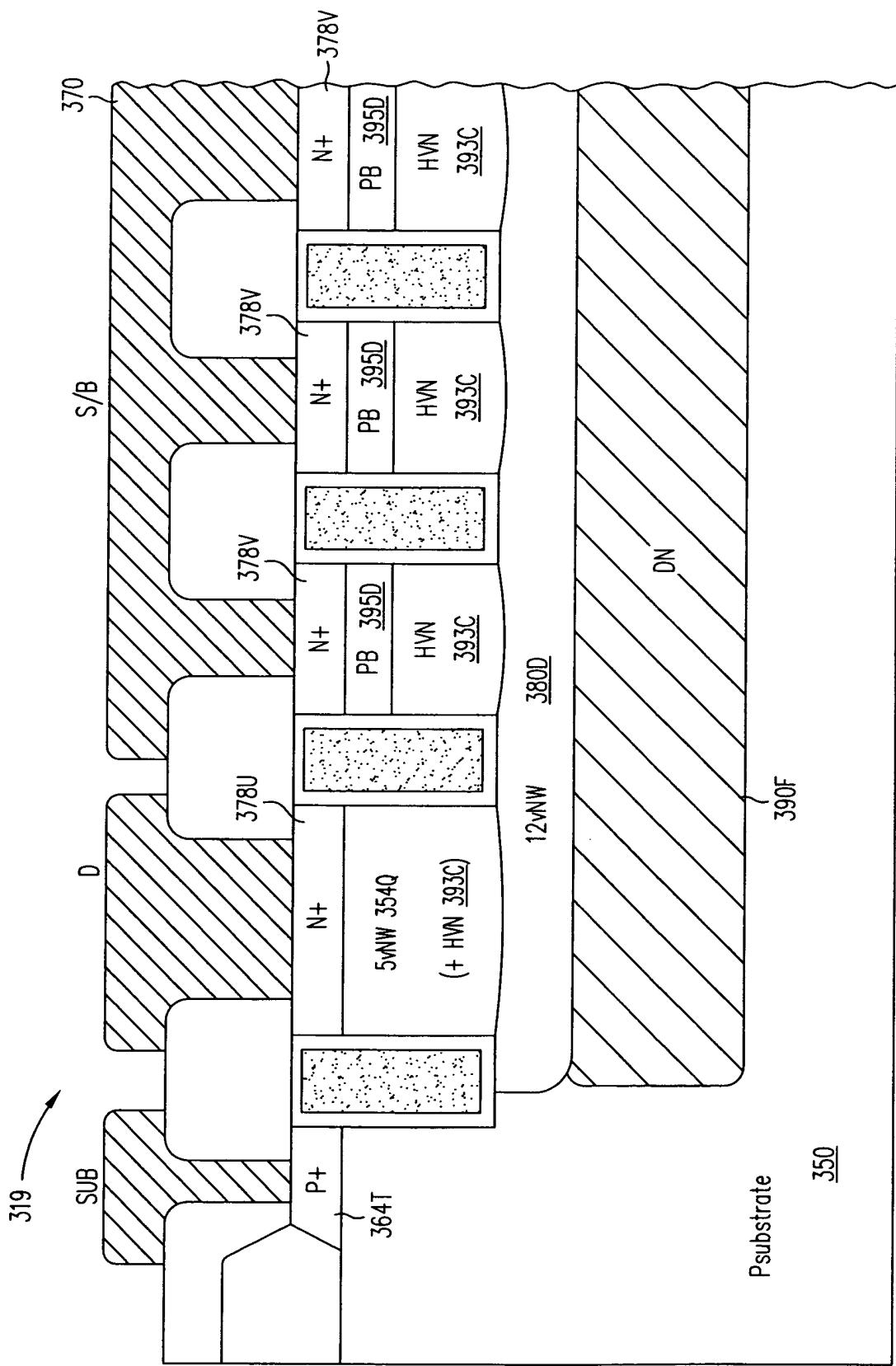


FIG. 18F

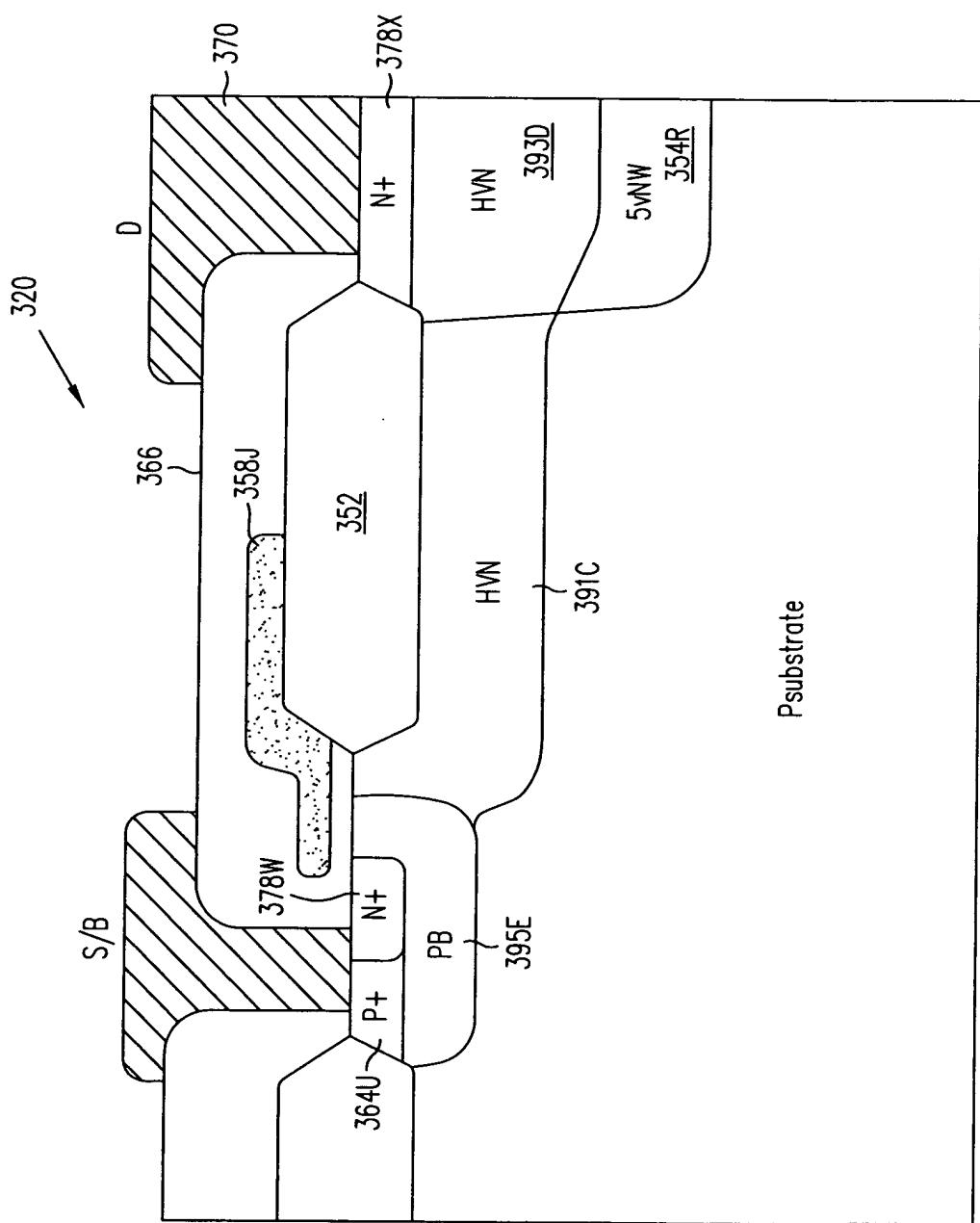


FIG. 18G

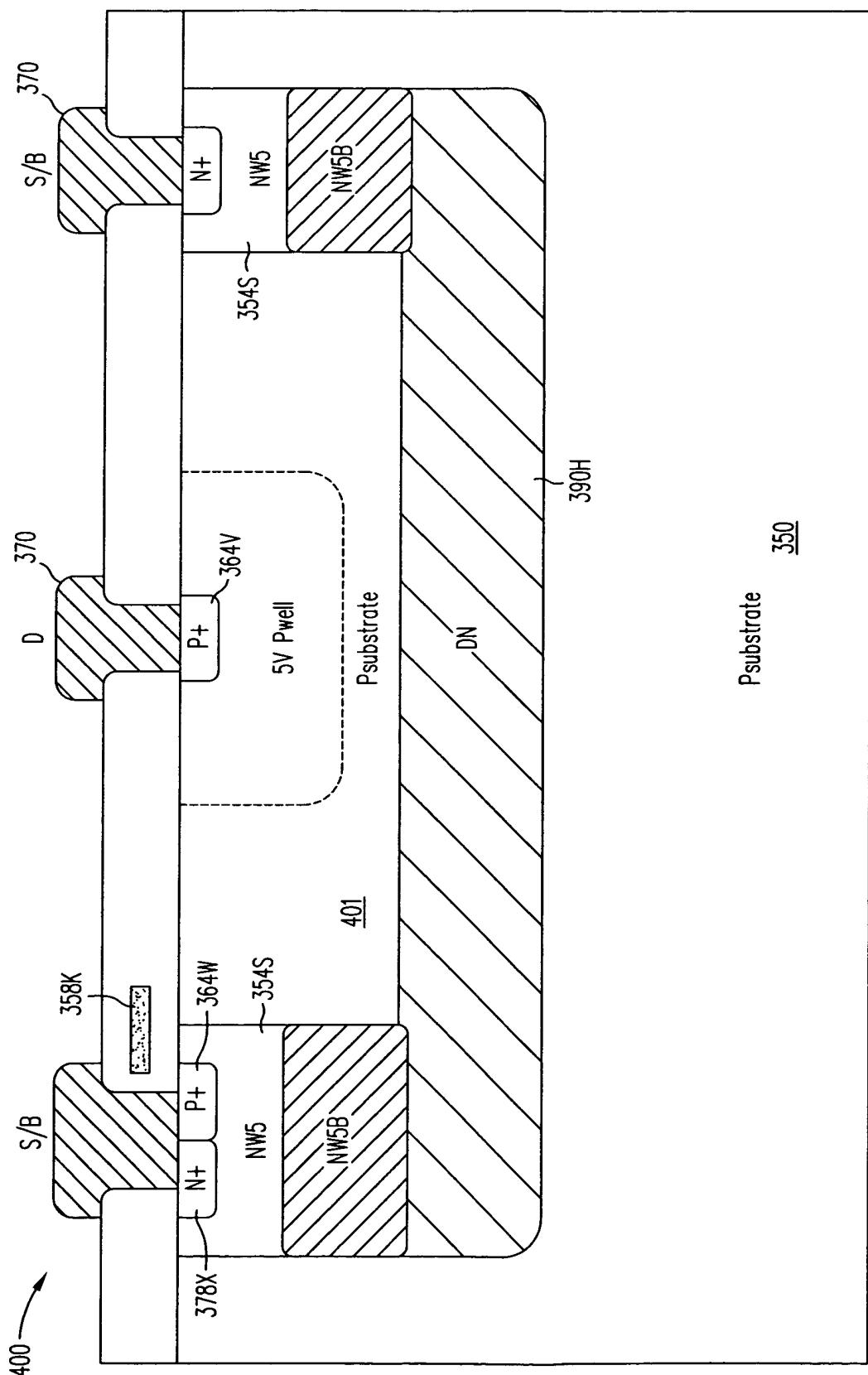
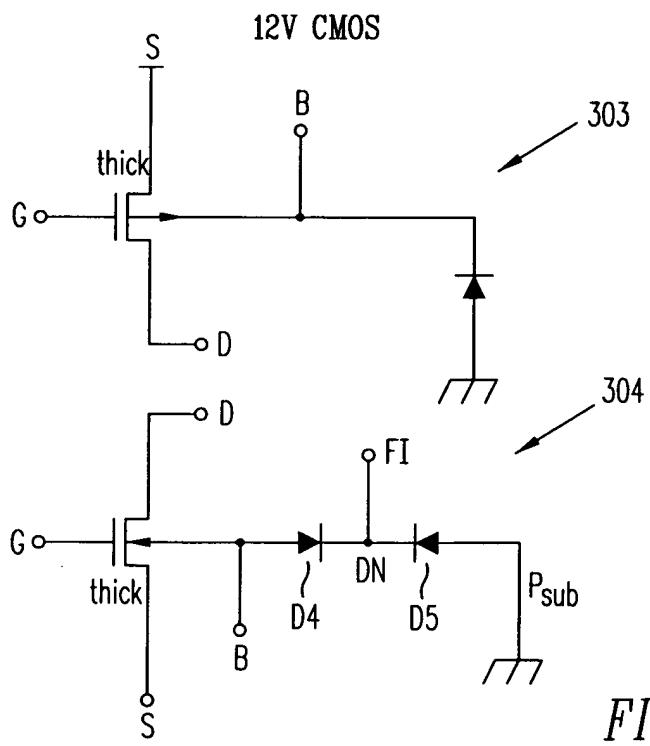
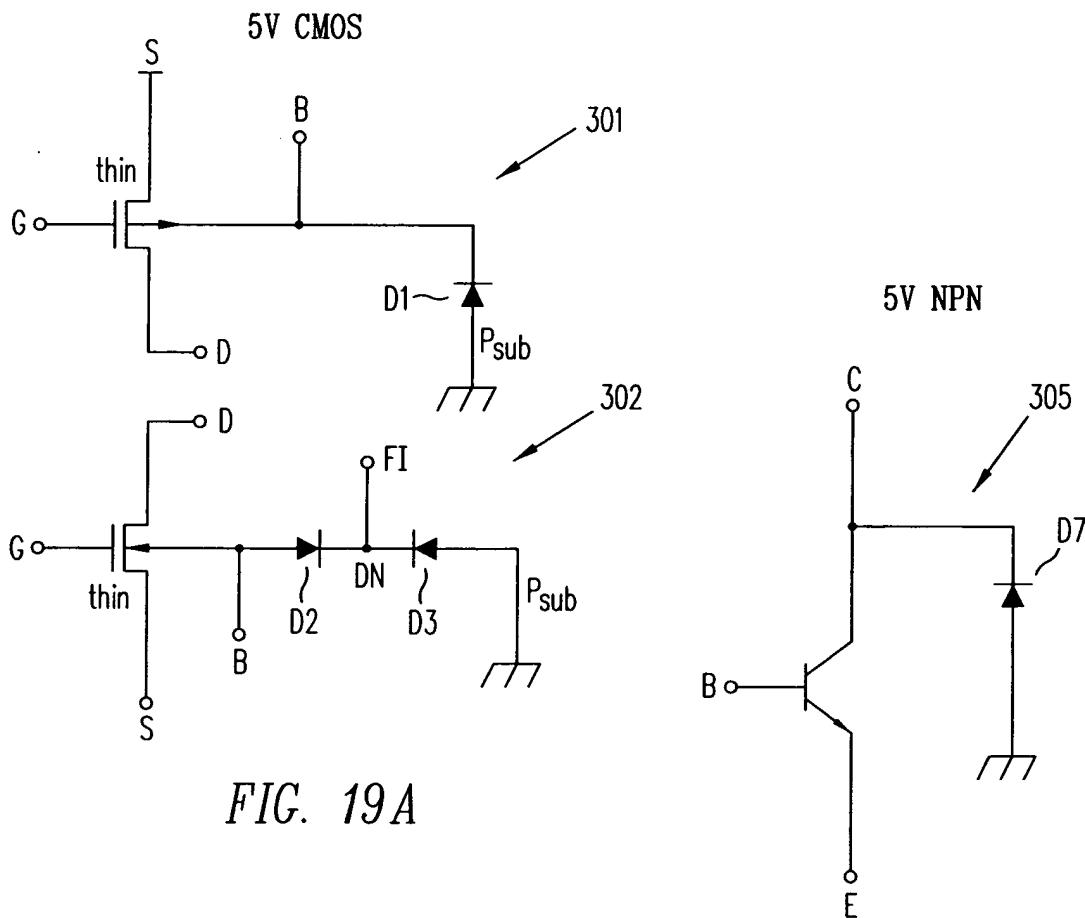


FIG. 18H

**FIG. 19B****FIG. 19C**

5V PNP

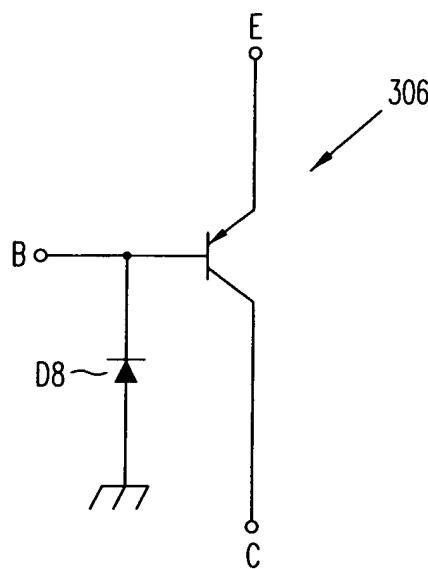


FIG. 19D

30V Trench LDMOS

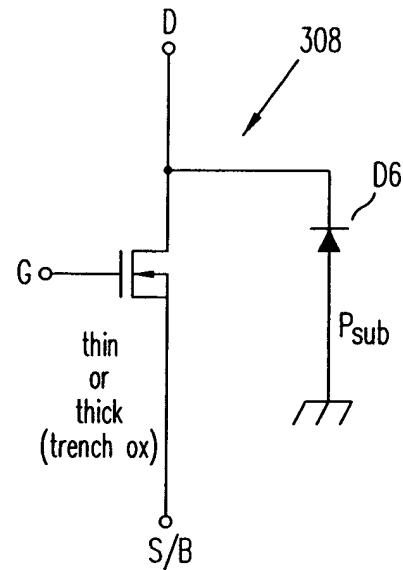


FIG. 19E

30V LDMOS

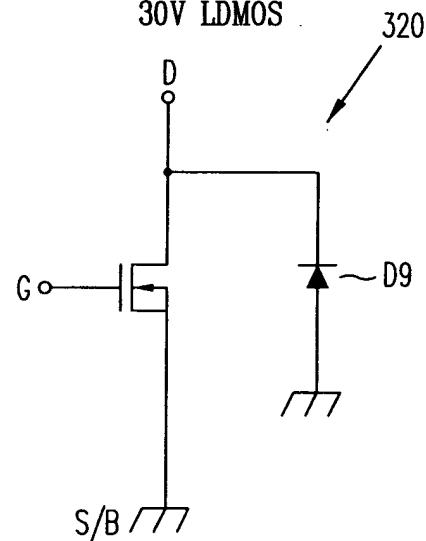
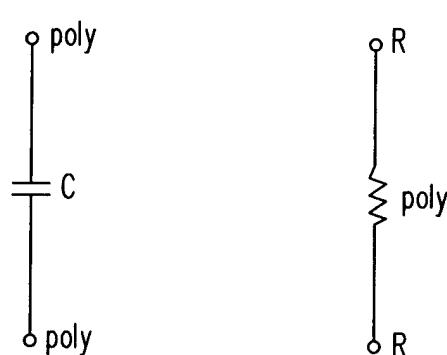
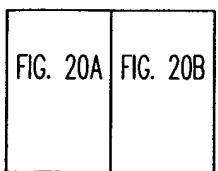


FIG. 19F

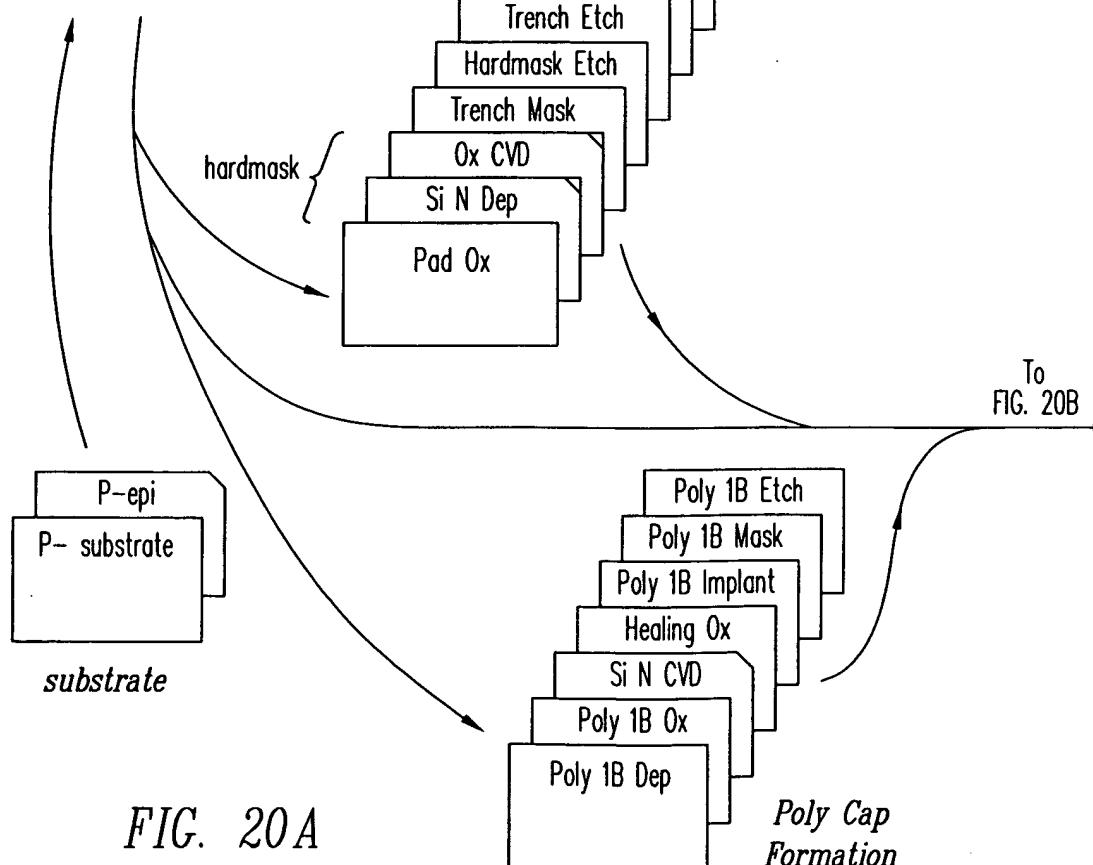
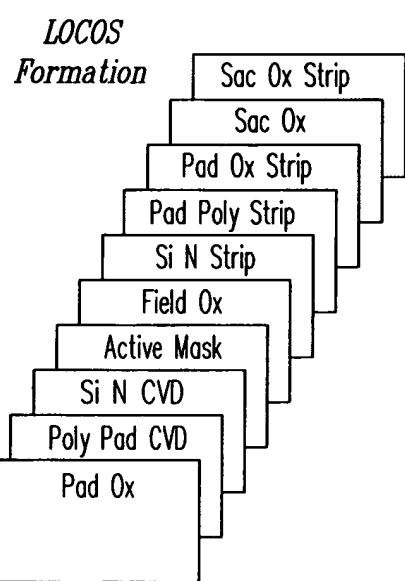
FIG. 19G

FIG. 19H





Key To
FIG. 20



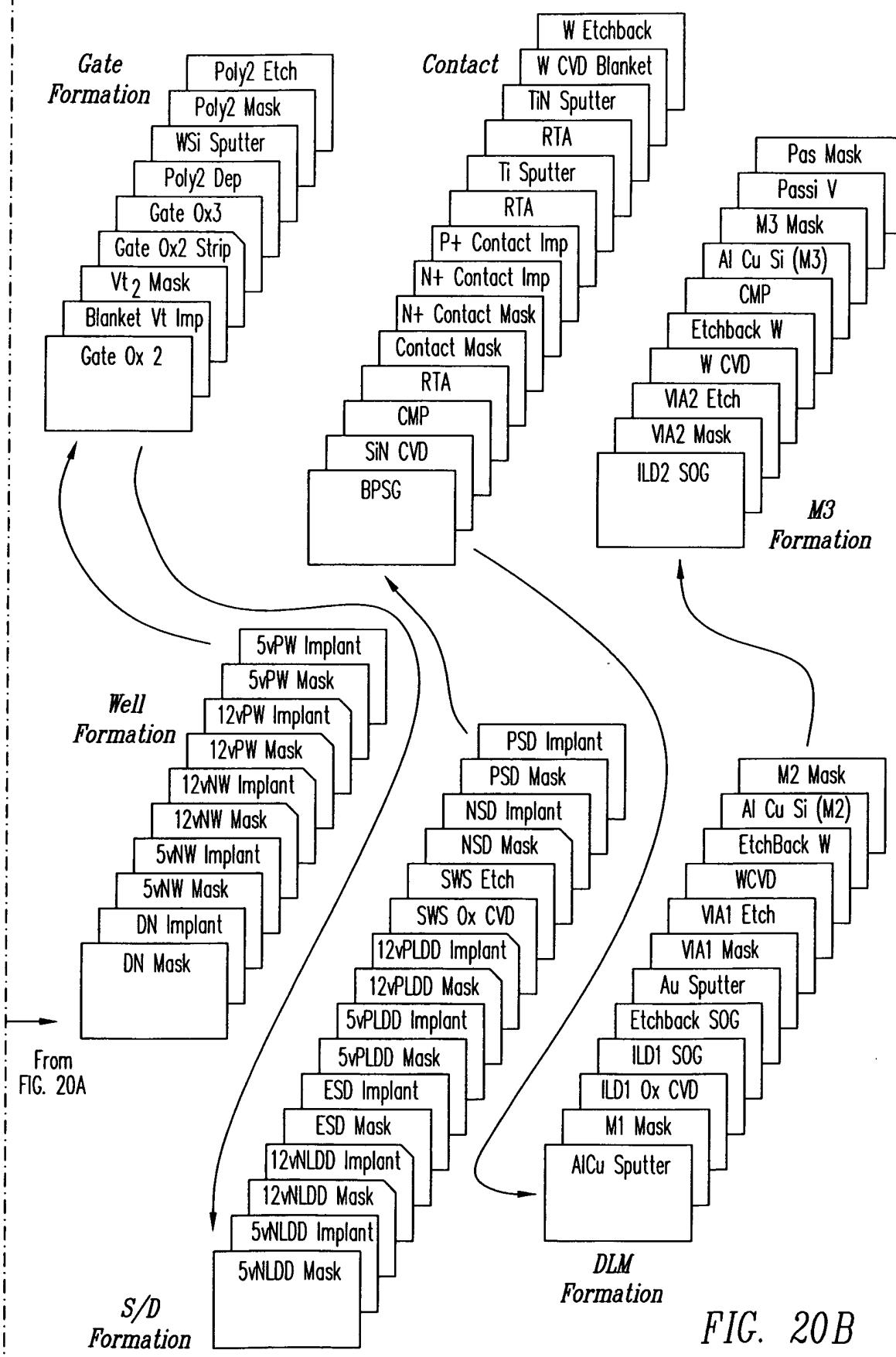
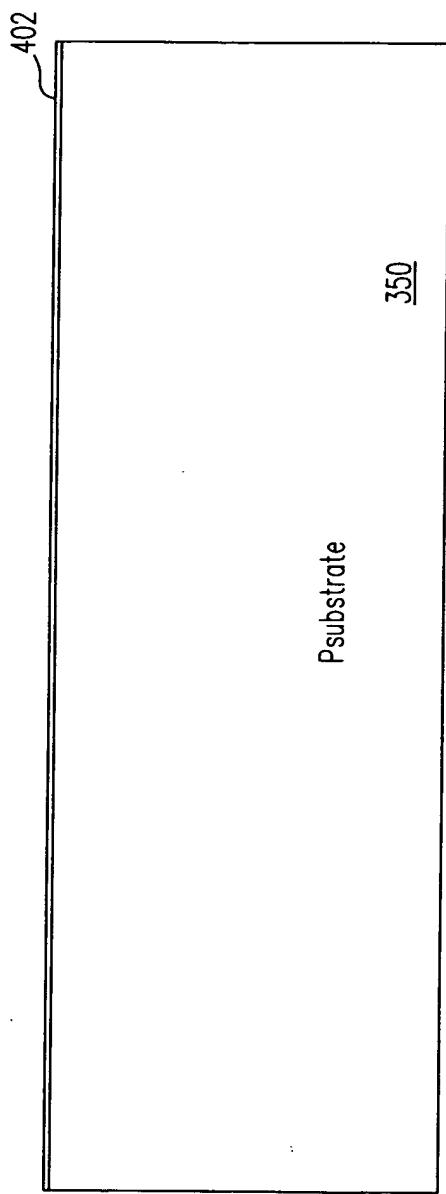


FIG. 20B

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FIG. 21



First Pad Oxide Layer

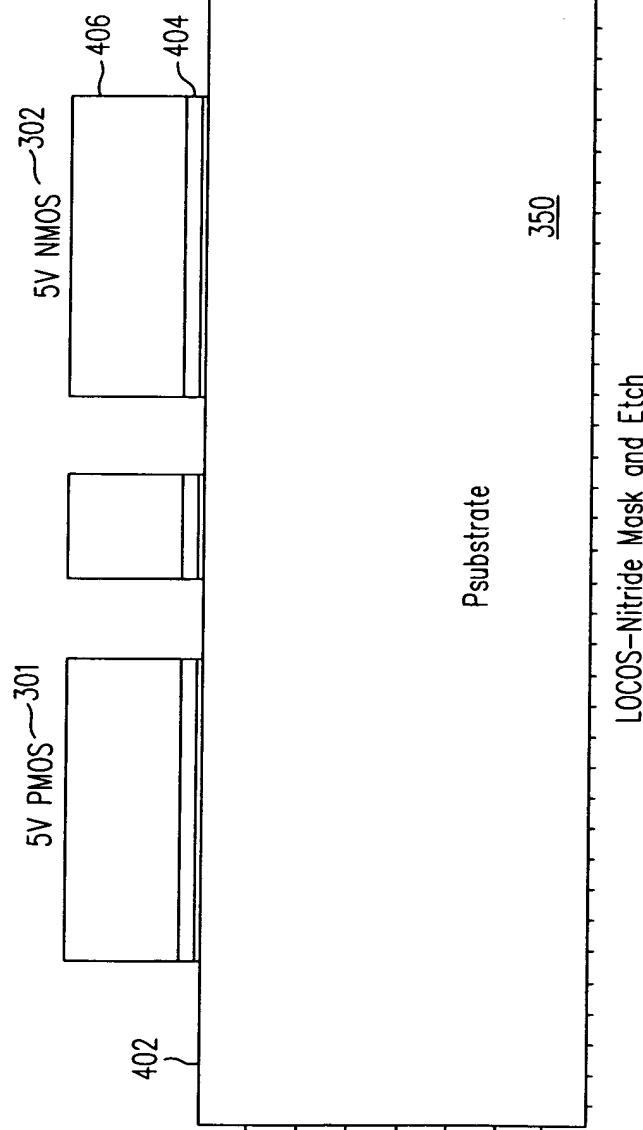


FIG. 22A

LOCOS-Nitride Mask and Etch

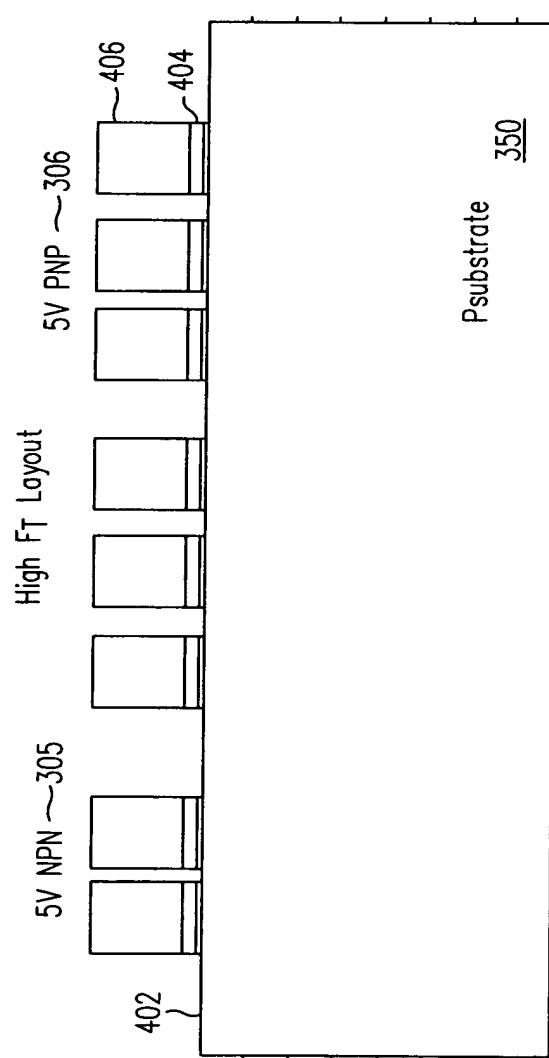


FIG. 22B

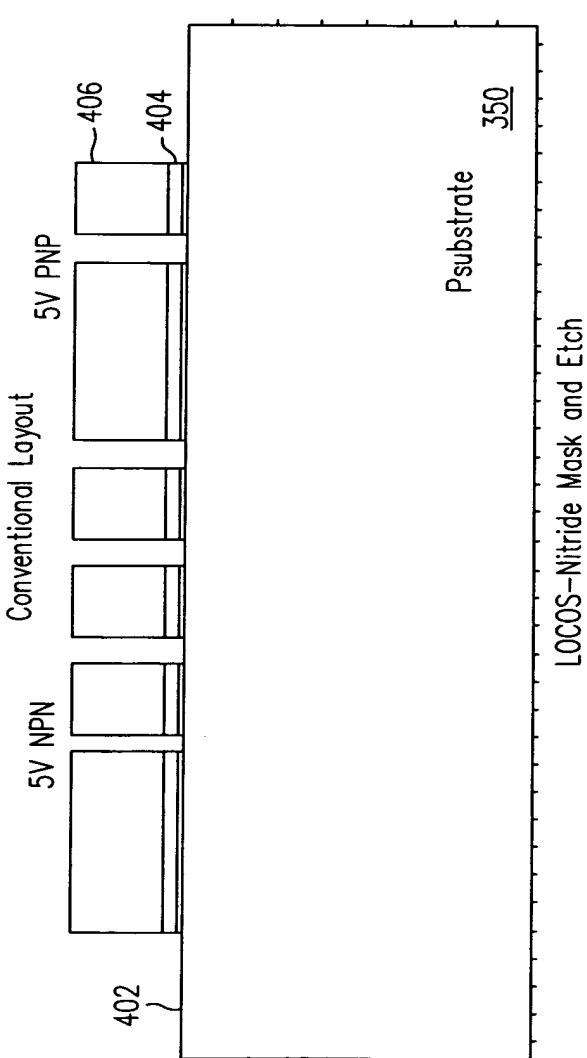
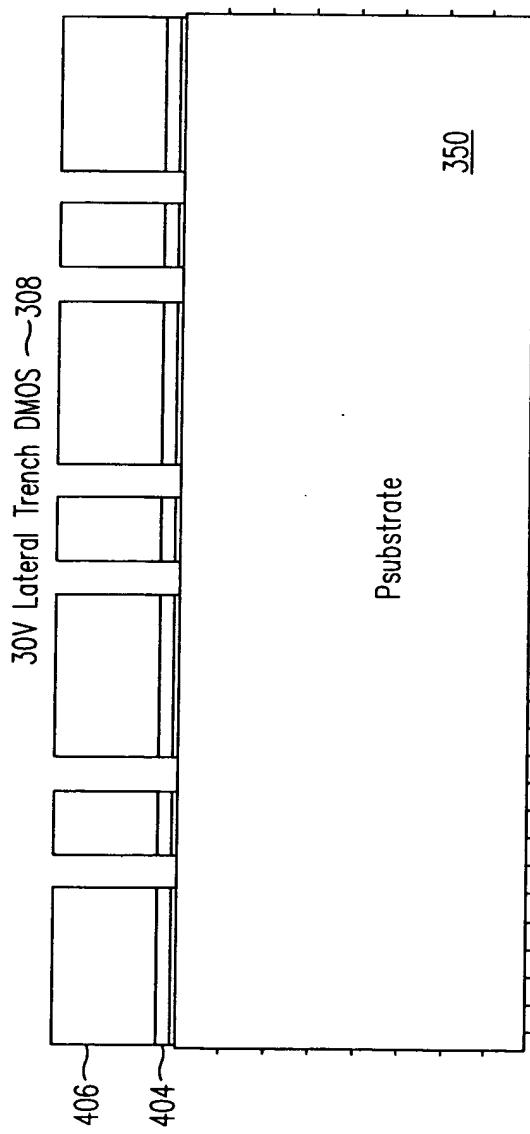


FIG. 22C

FIG. 22D



LOCOS-Nitride Mask and Etch
309 ~ 12V PMOS Symmetrical 12V CMOS

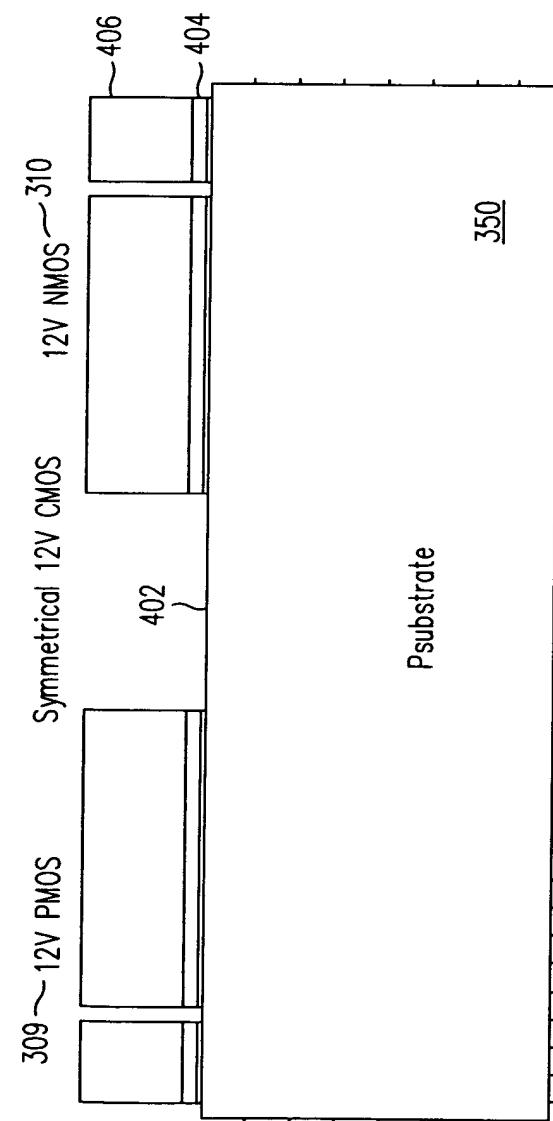


FIG. 22E

LOCOS-Nitride Mask and Etch

FIG. 23A

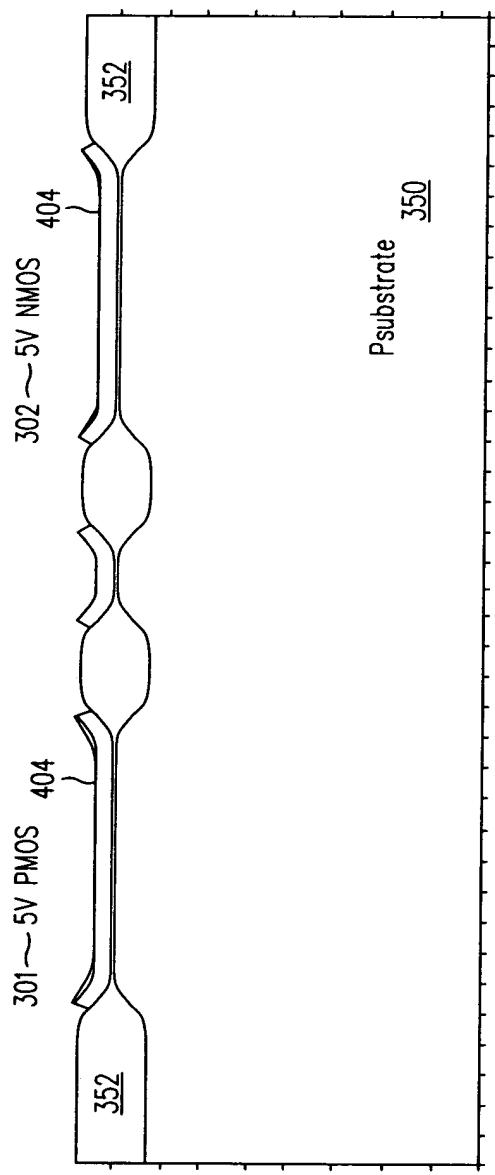
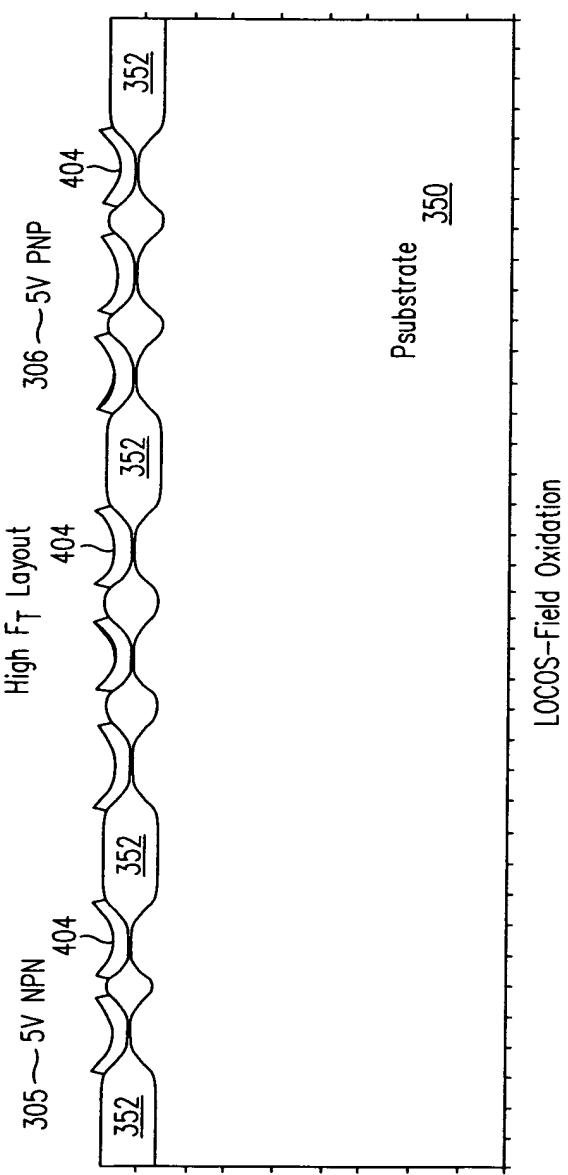


FIG. 23B



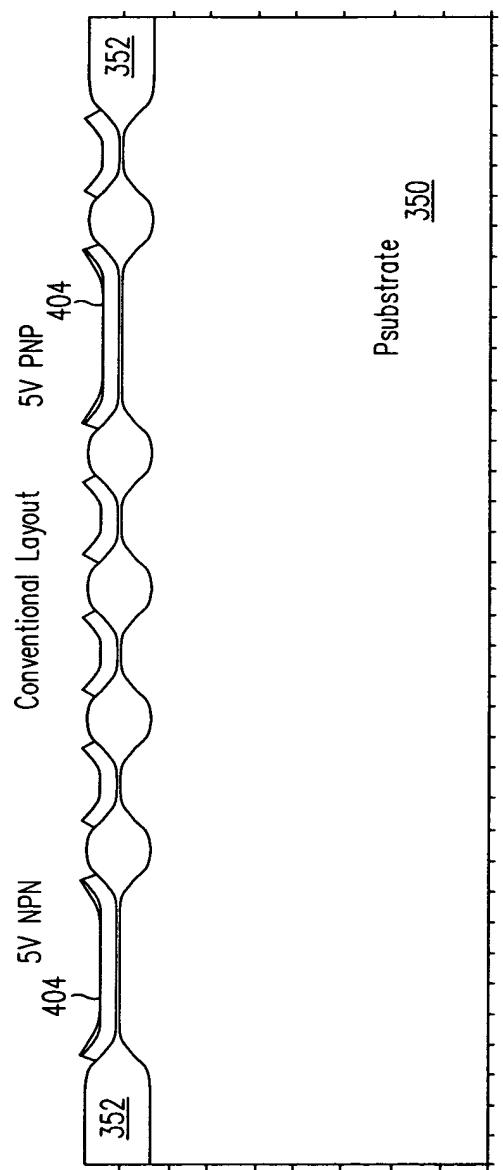


FIG. 23C

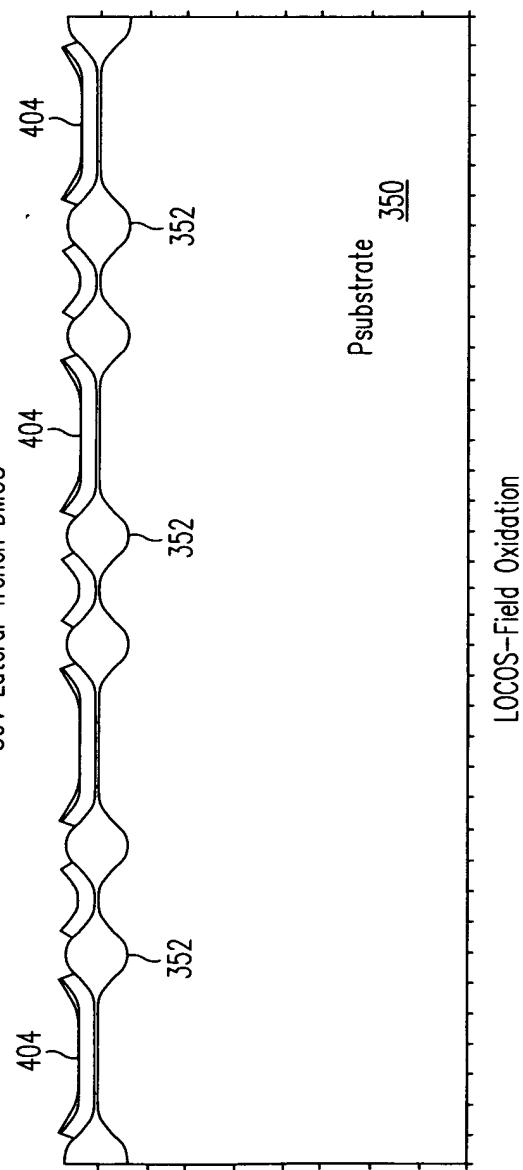


FIG. 23D

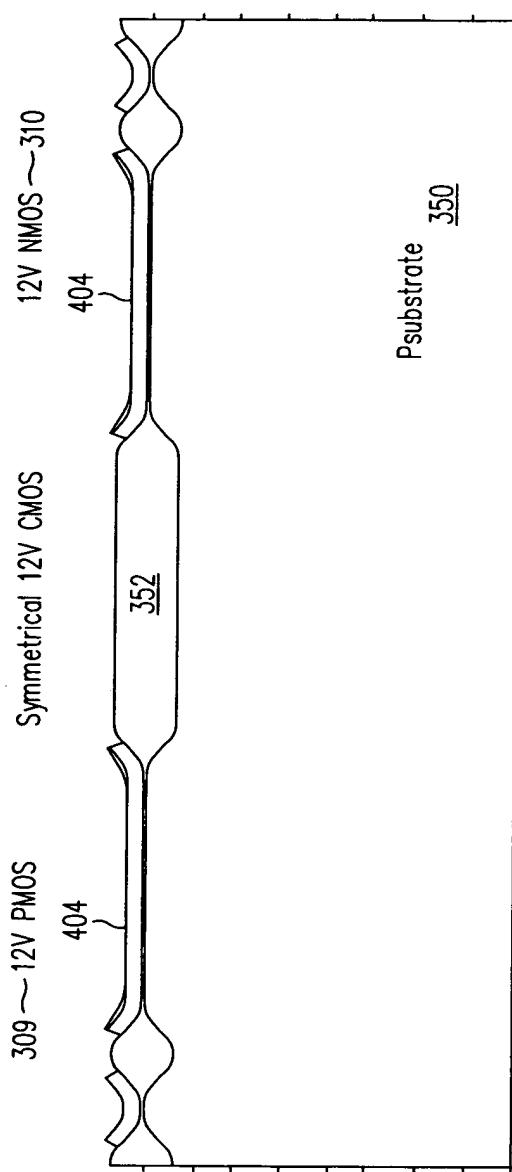


FIG. 23E

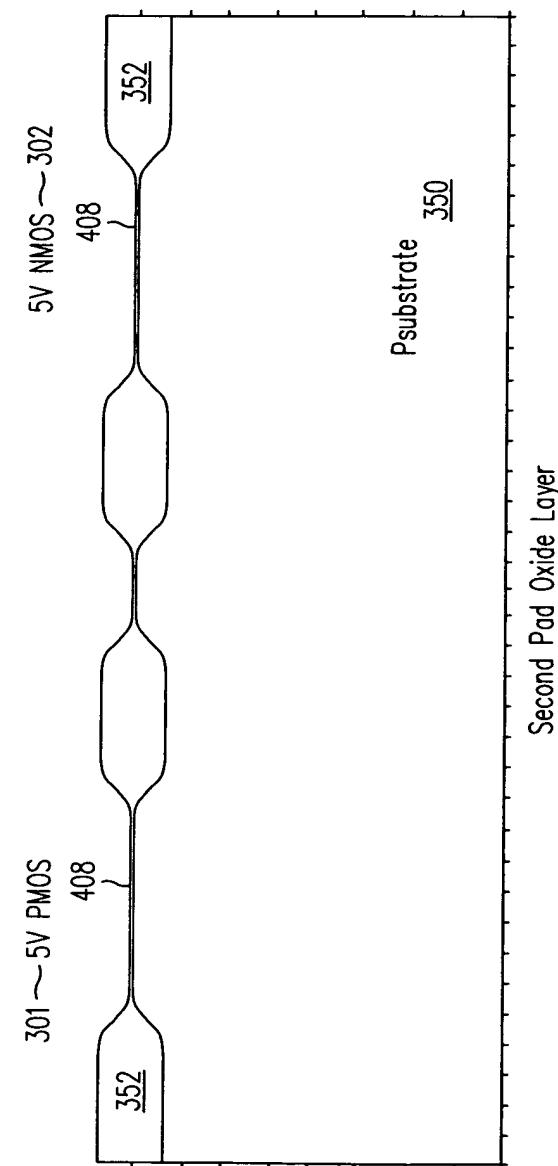


FIG. 24A

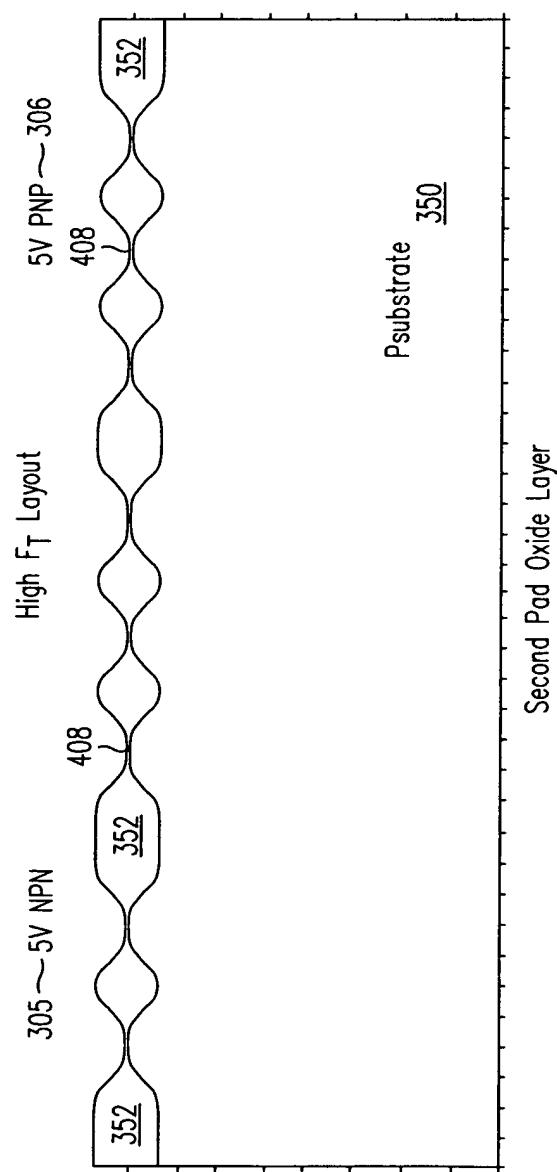


FIG. 24B

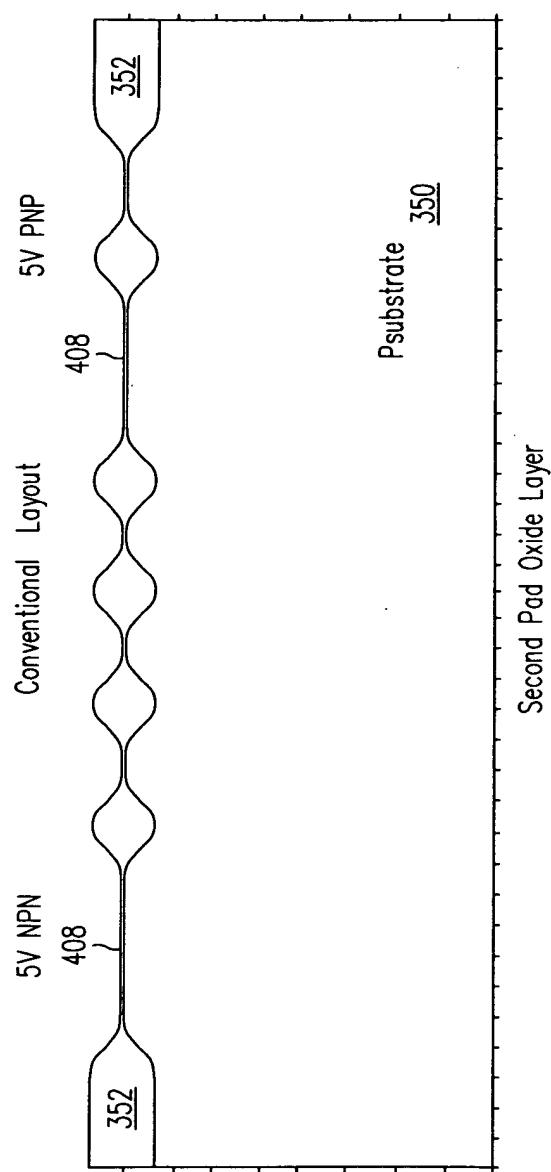


FIG. 24C

FIG. 24D

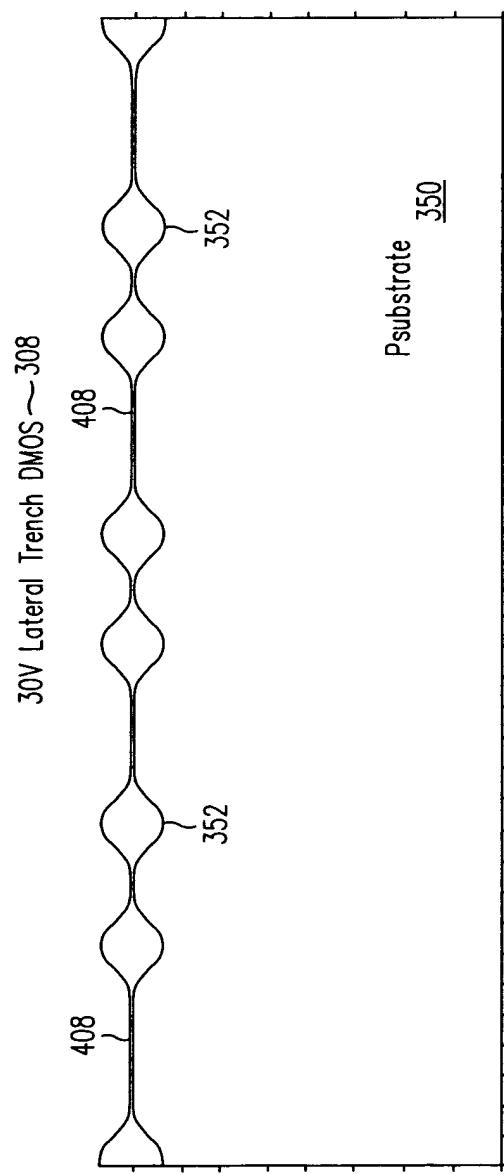
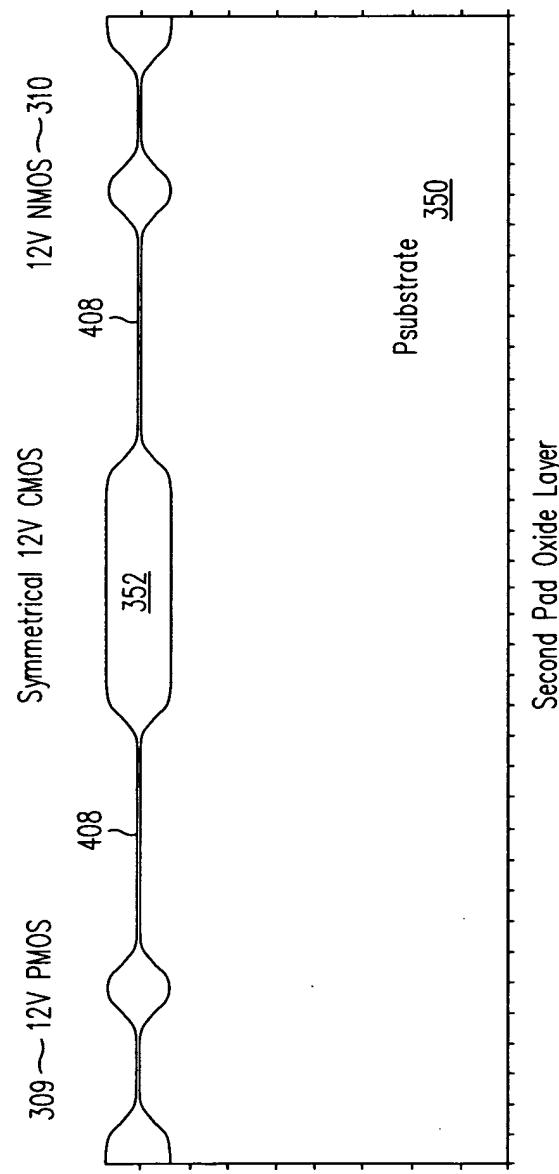


FIG. 24E



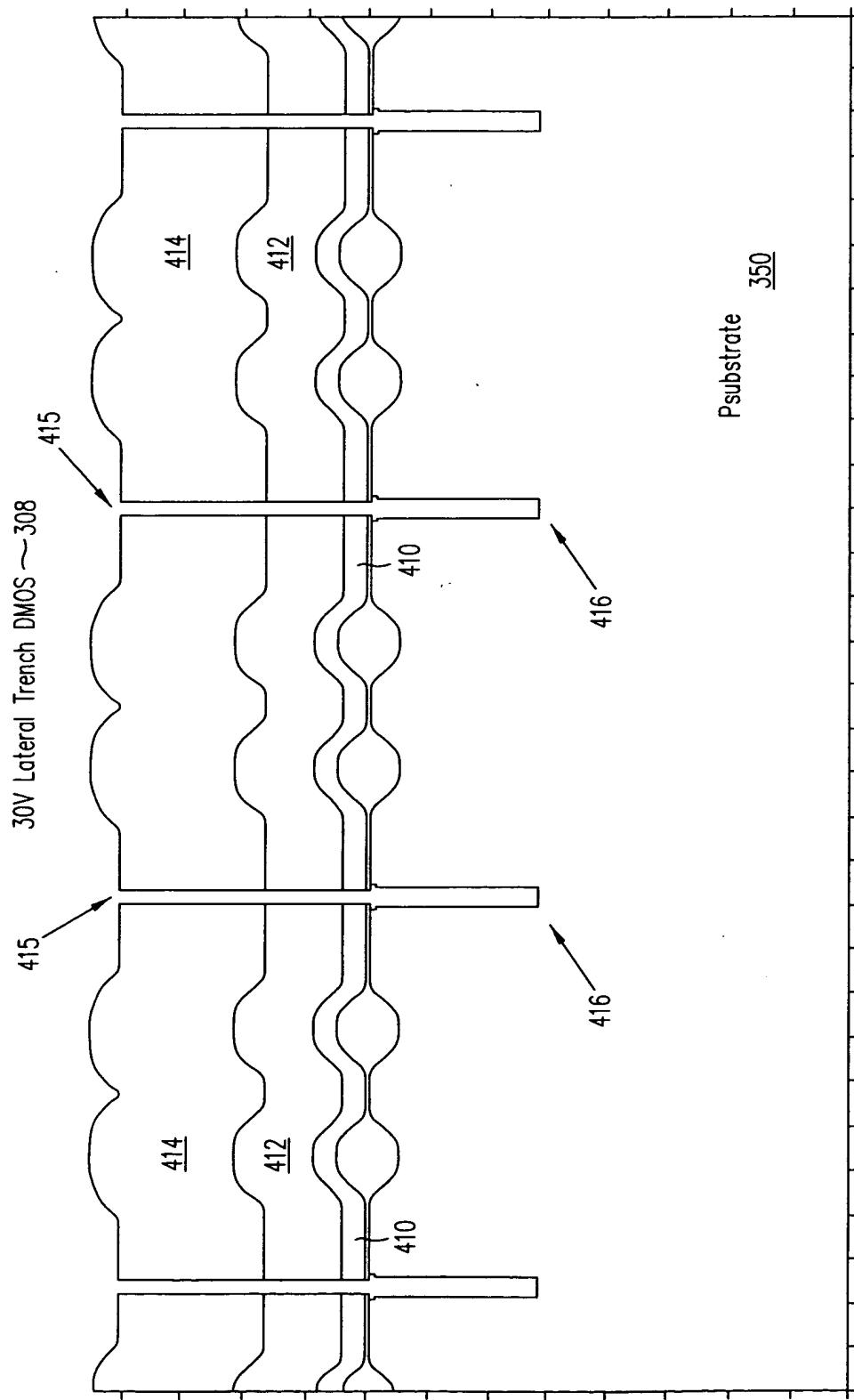


FIG. 25D

Trench Hard Mask

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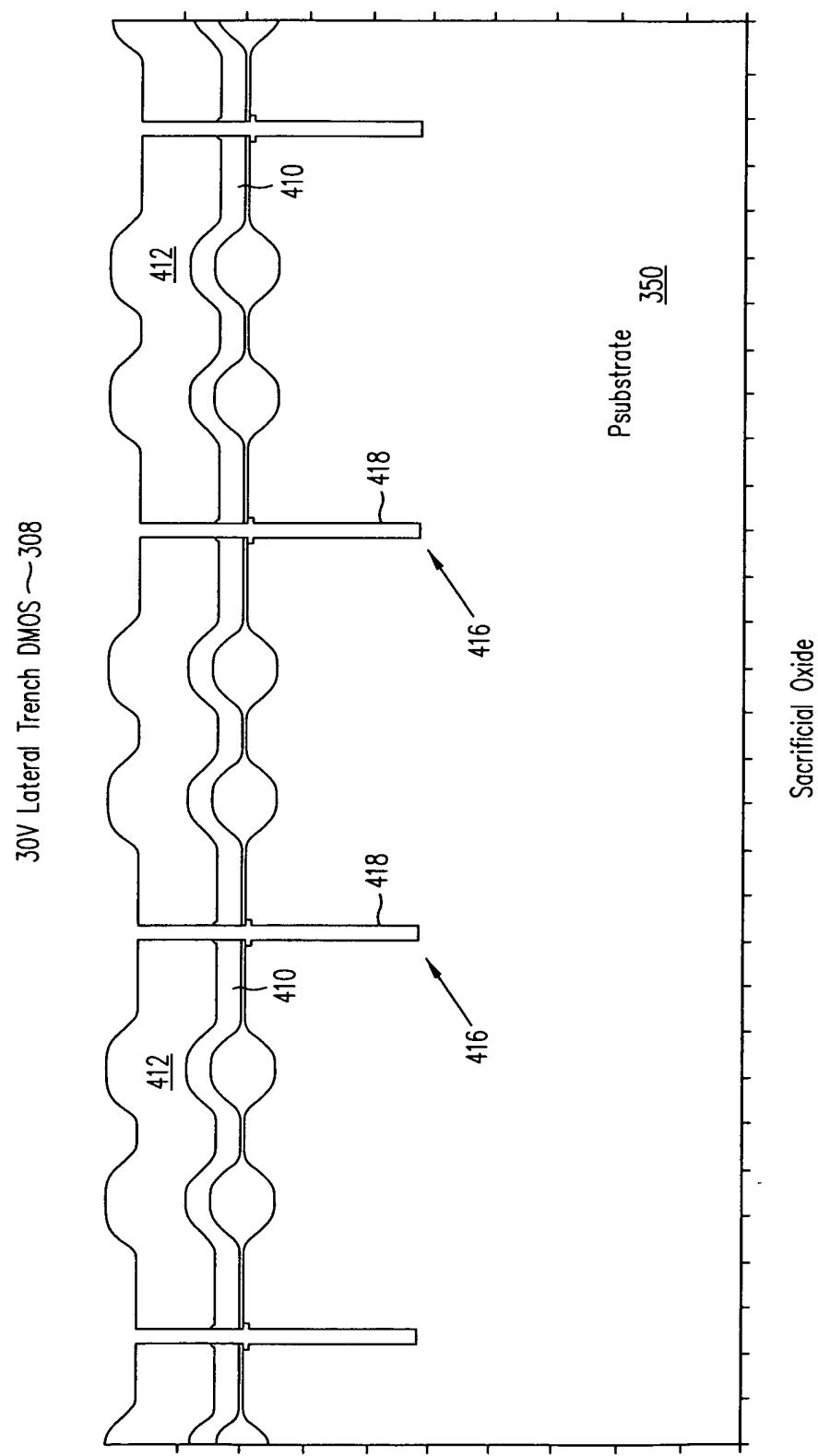


FIG. 26D

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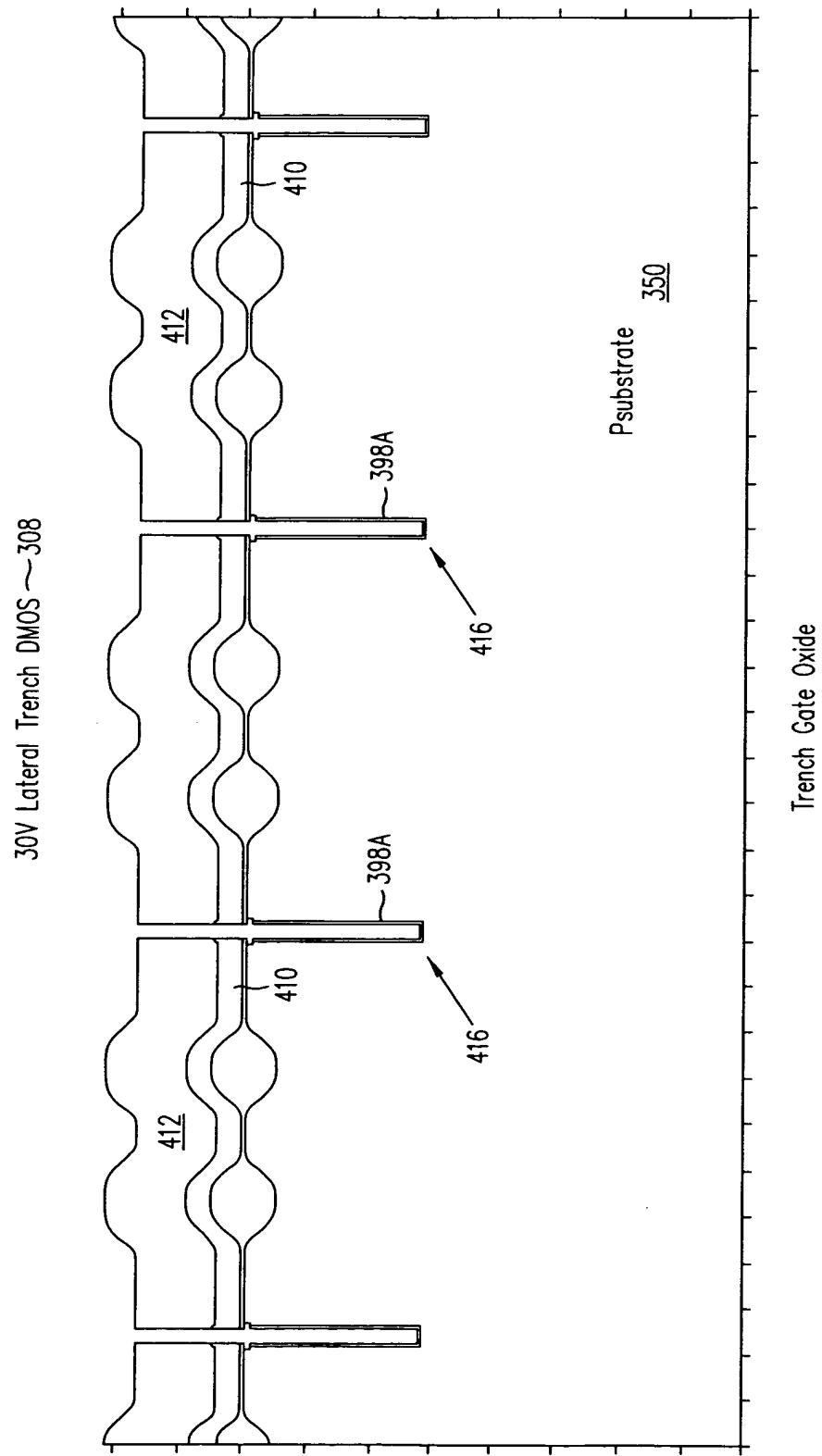
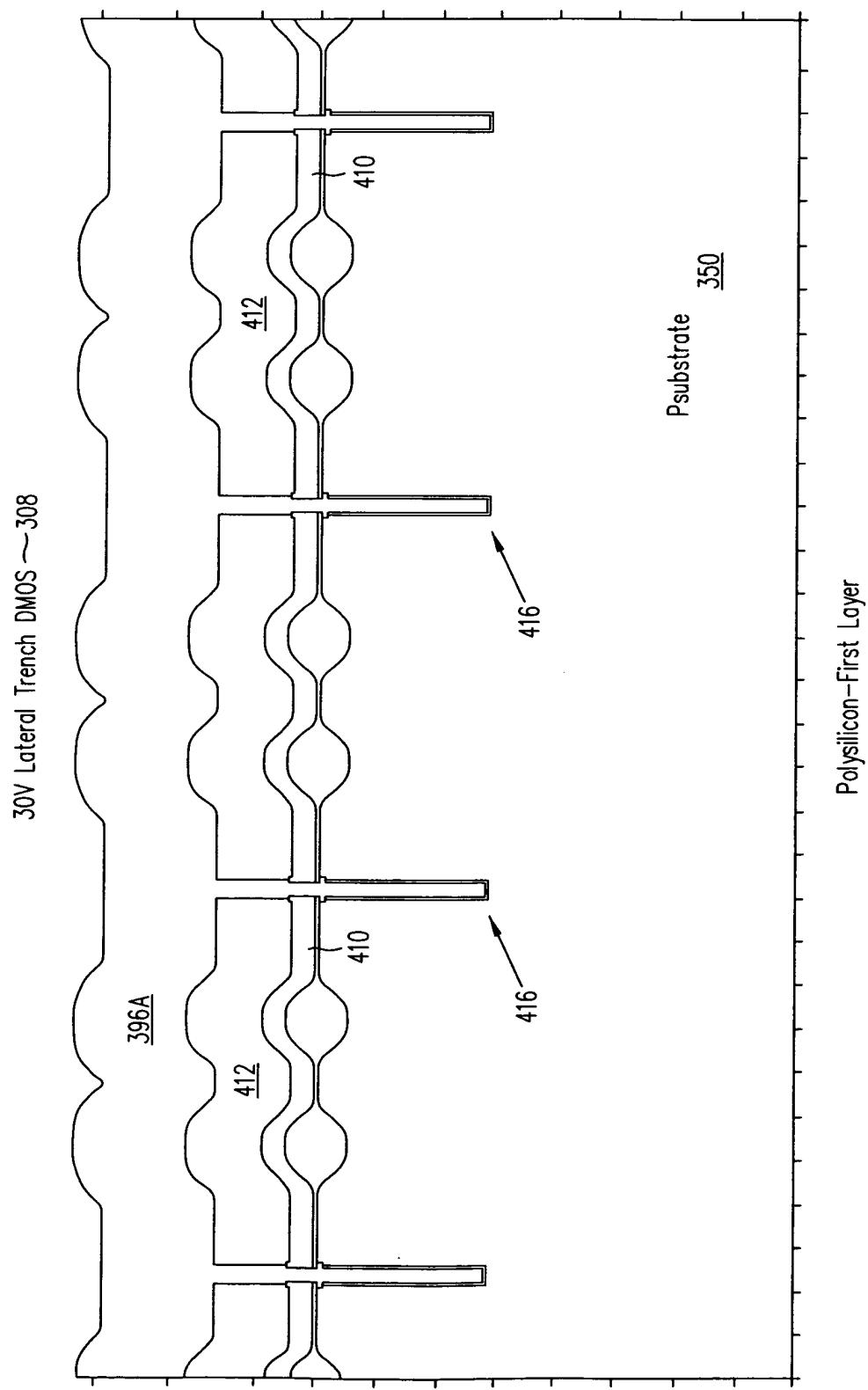
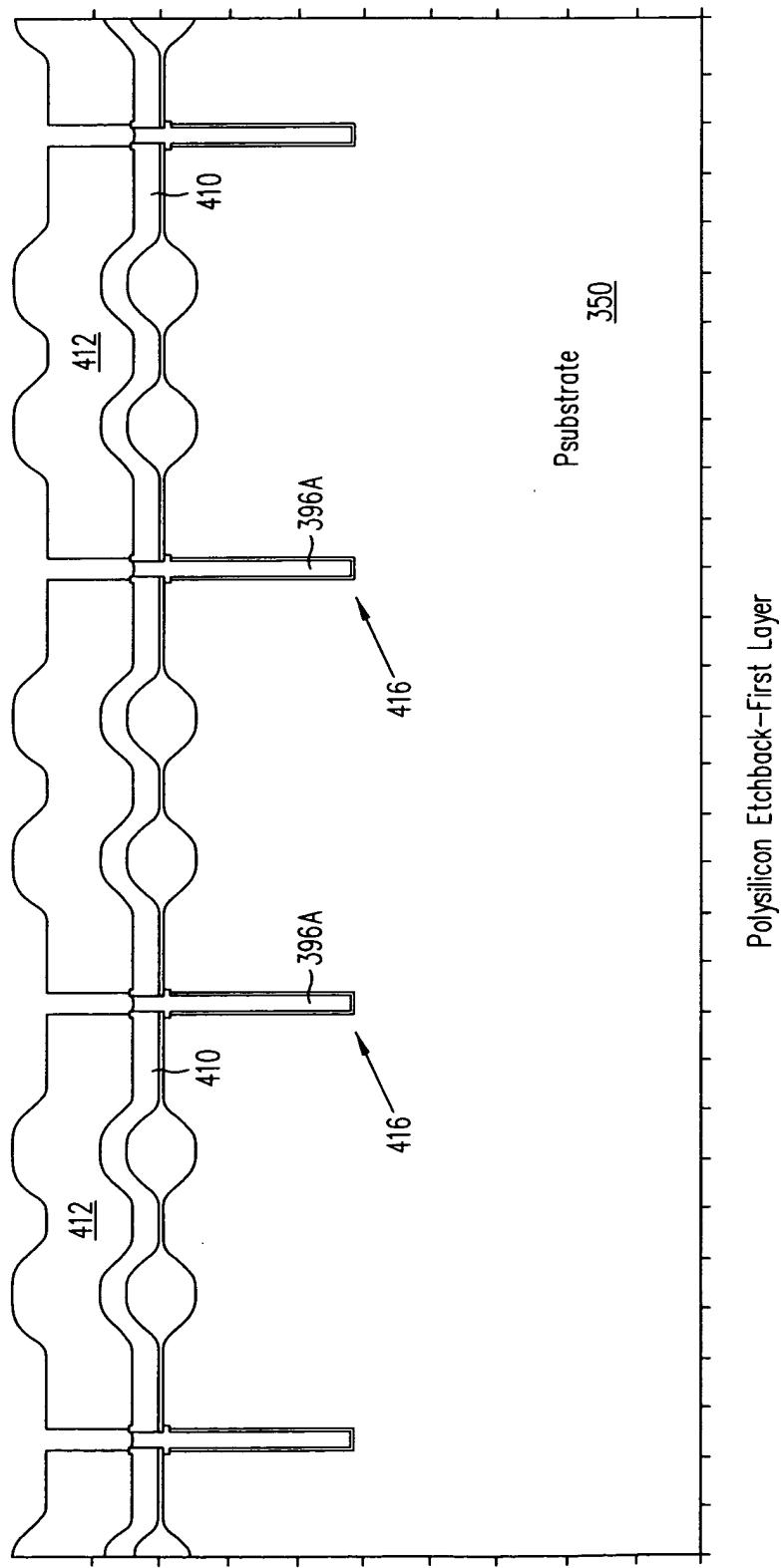


FIG. 27D



30V Lateral Trench DMOS ~308

30V Lateral Trench DMOS ~308



Polysilicon Etchback-First Layer

FIG. 29D

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30V Lateral Trench DMOS ~308

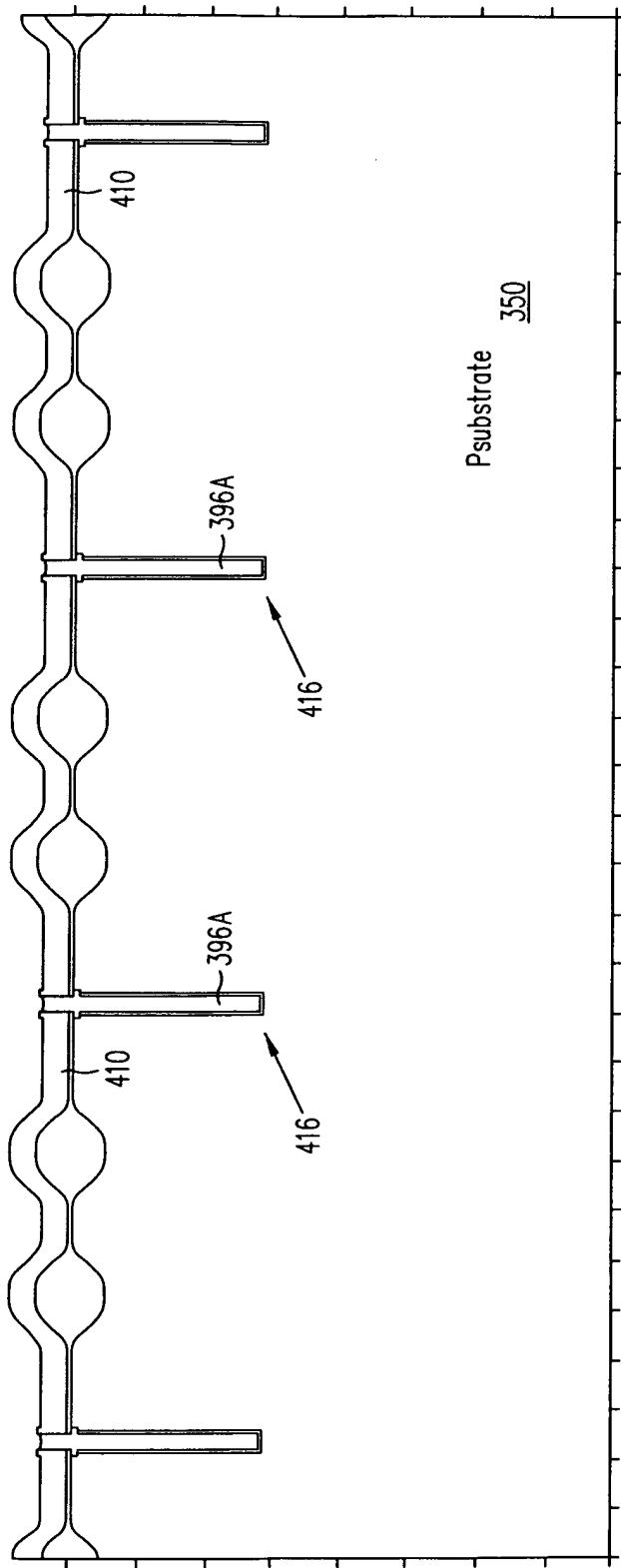
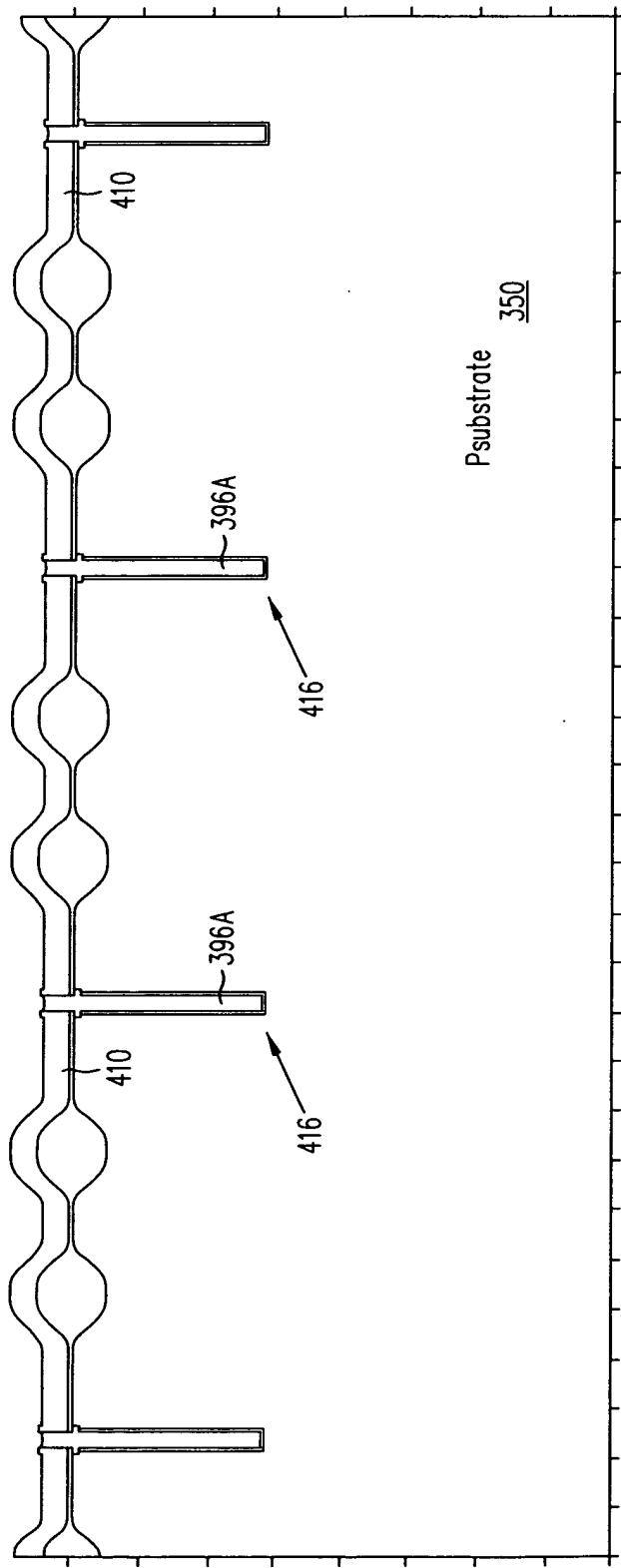


FIG. 30D

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30V Lateral Trench DMOS ~308



Second Polysilicon Etchback-First Layer

FIG. 31D

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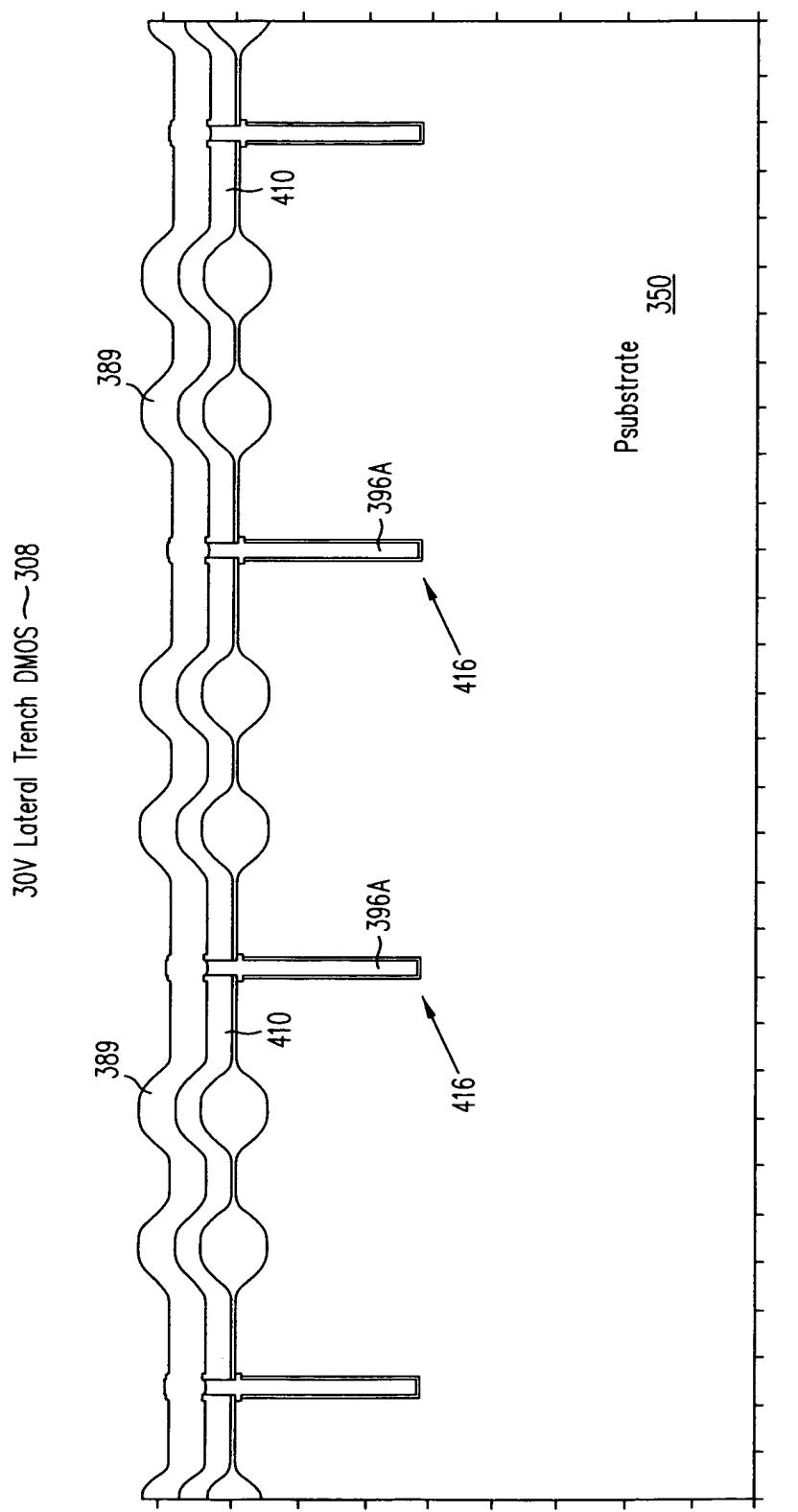


FIG. 32D

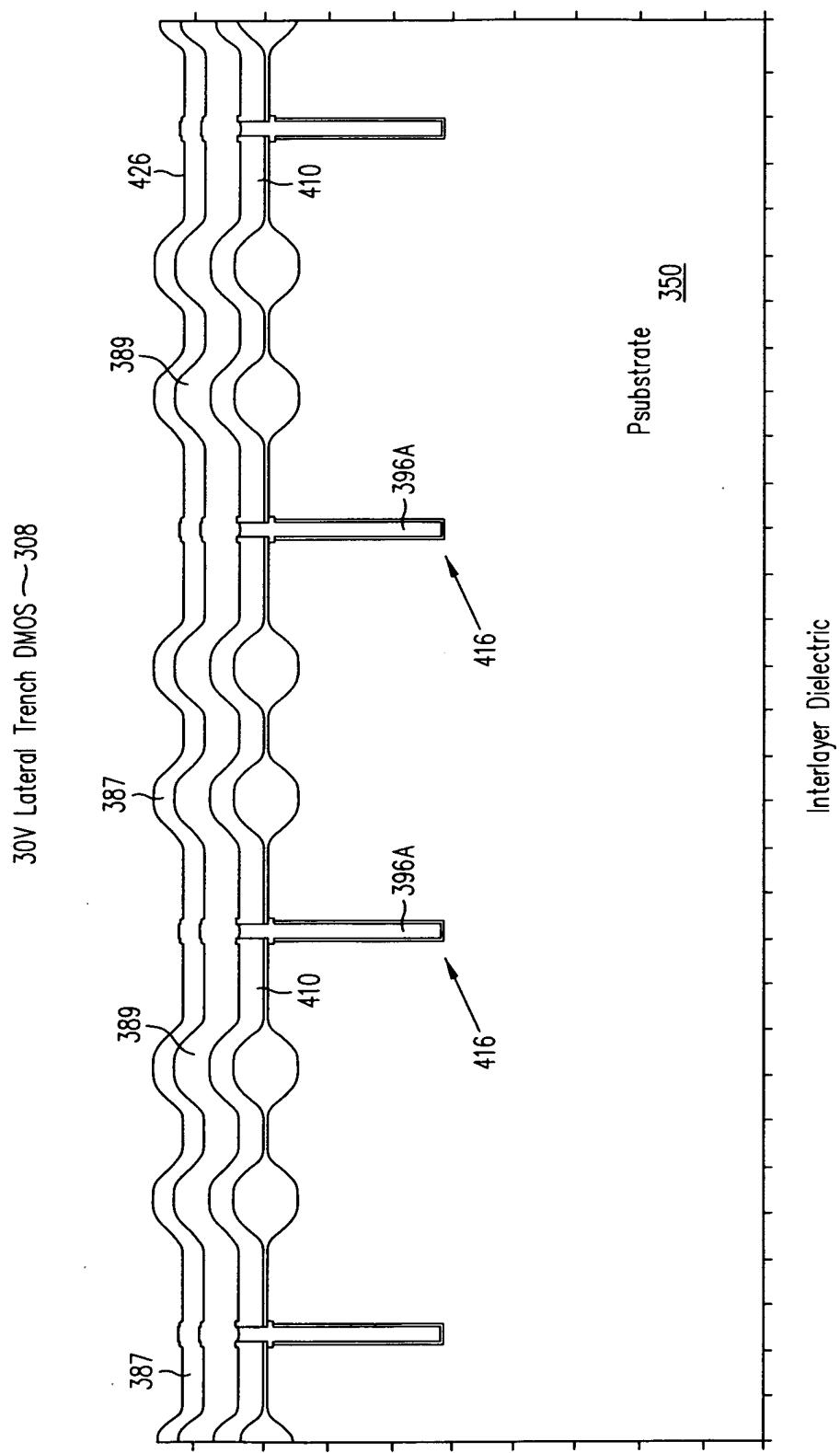


FIG. 33D

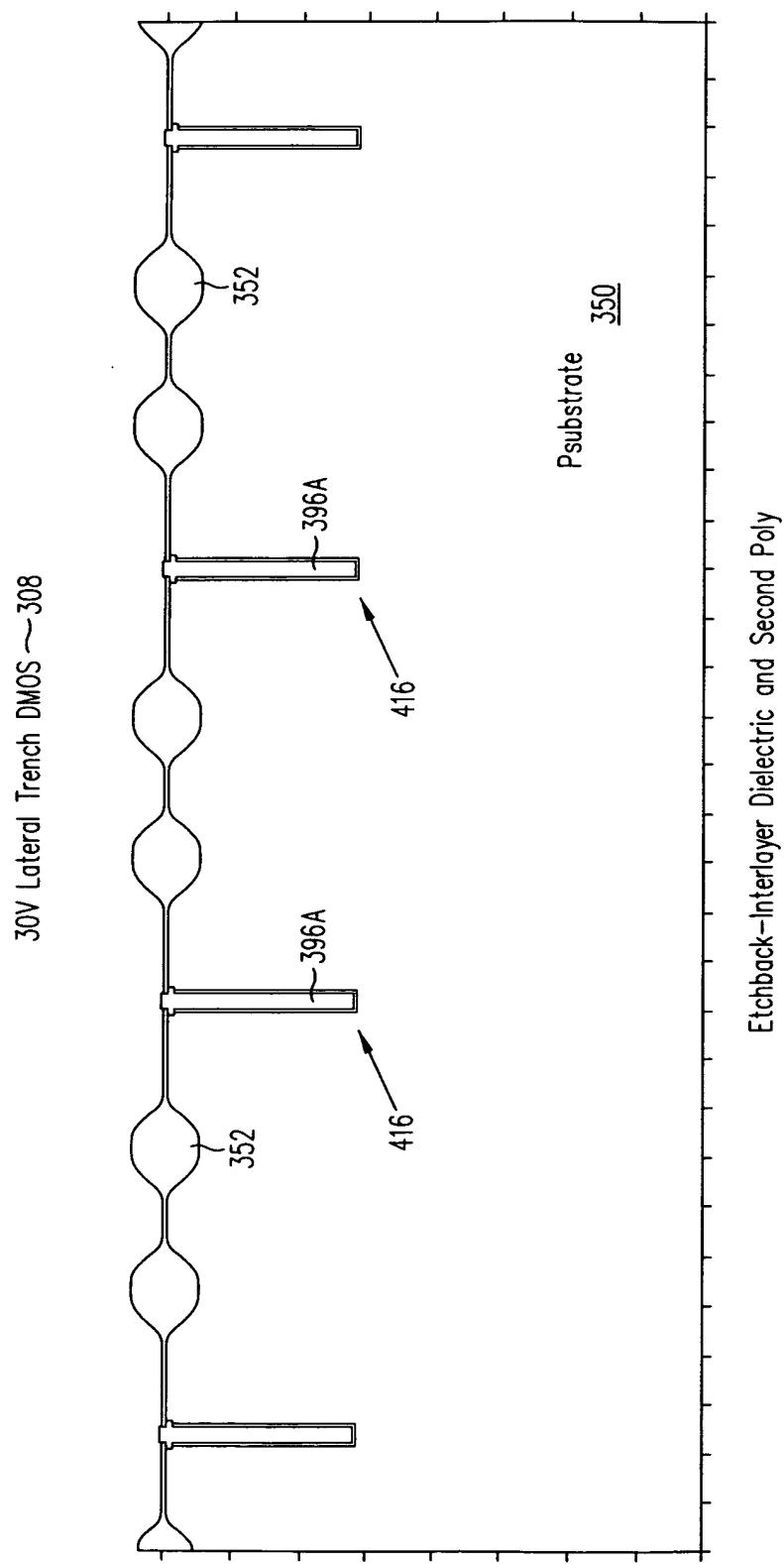


FIG. 34D

Etchback-Interlayer Dielectric and Second Poly

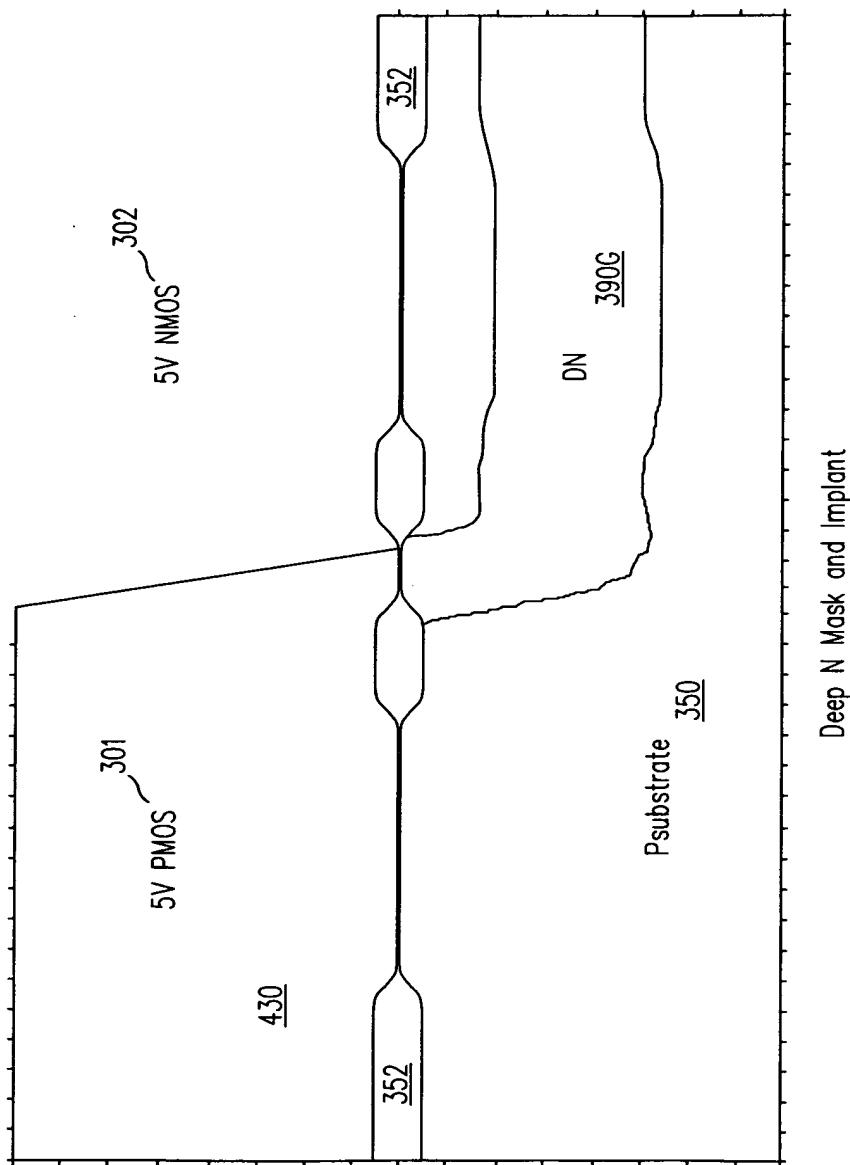
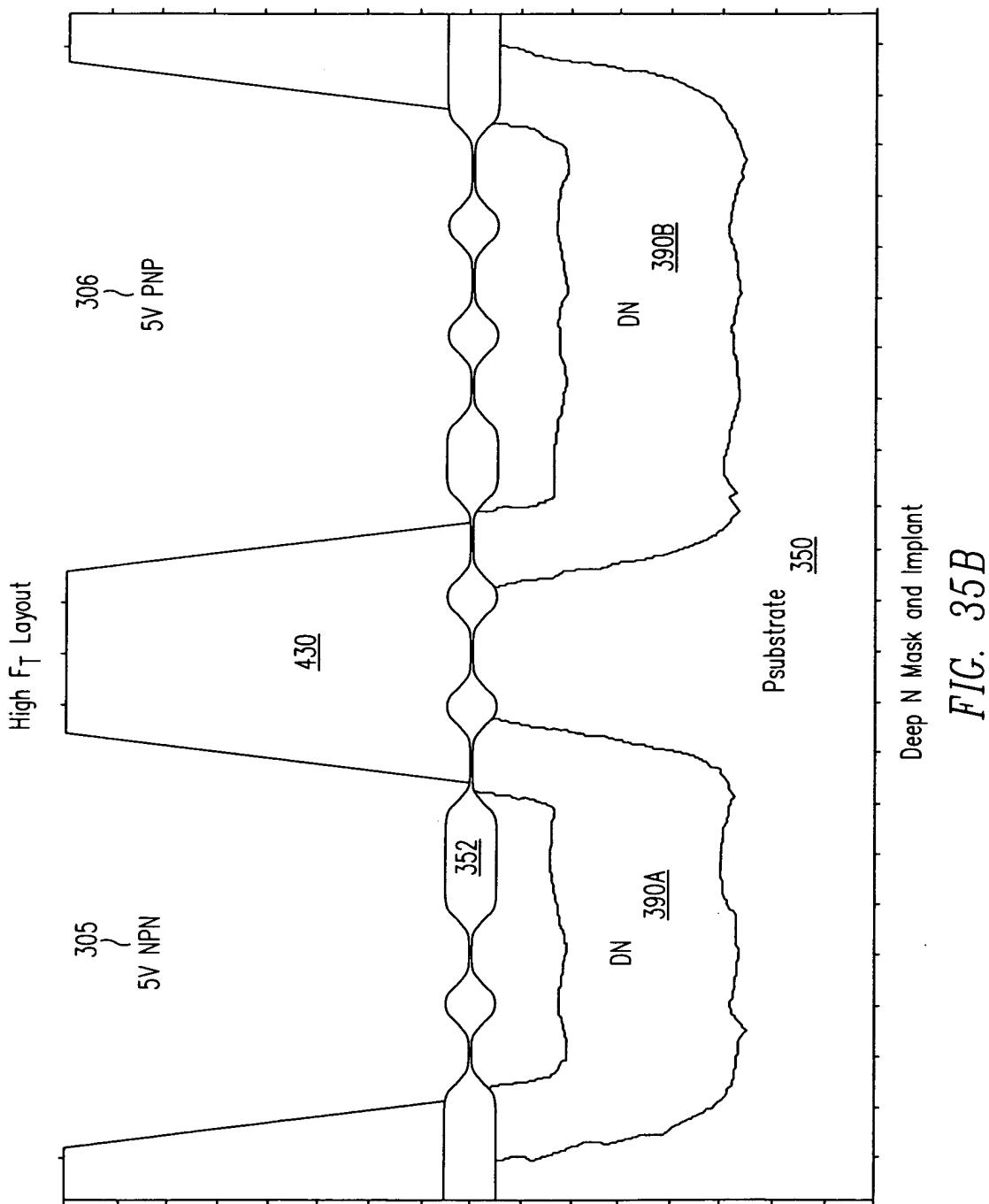
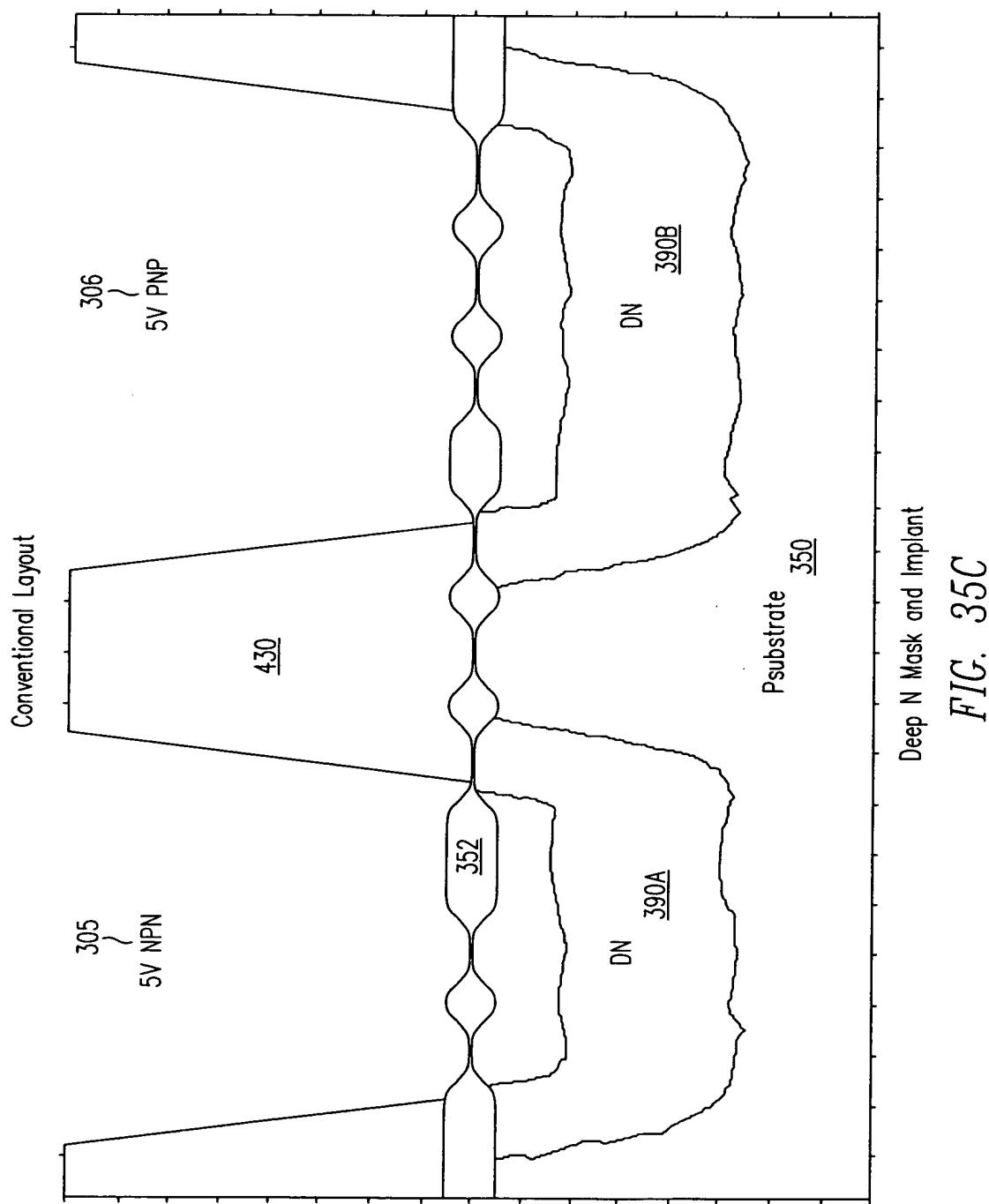


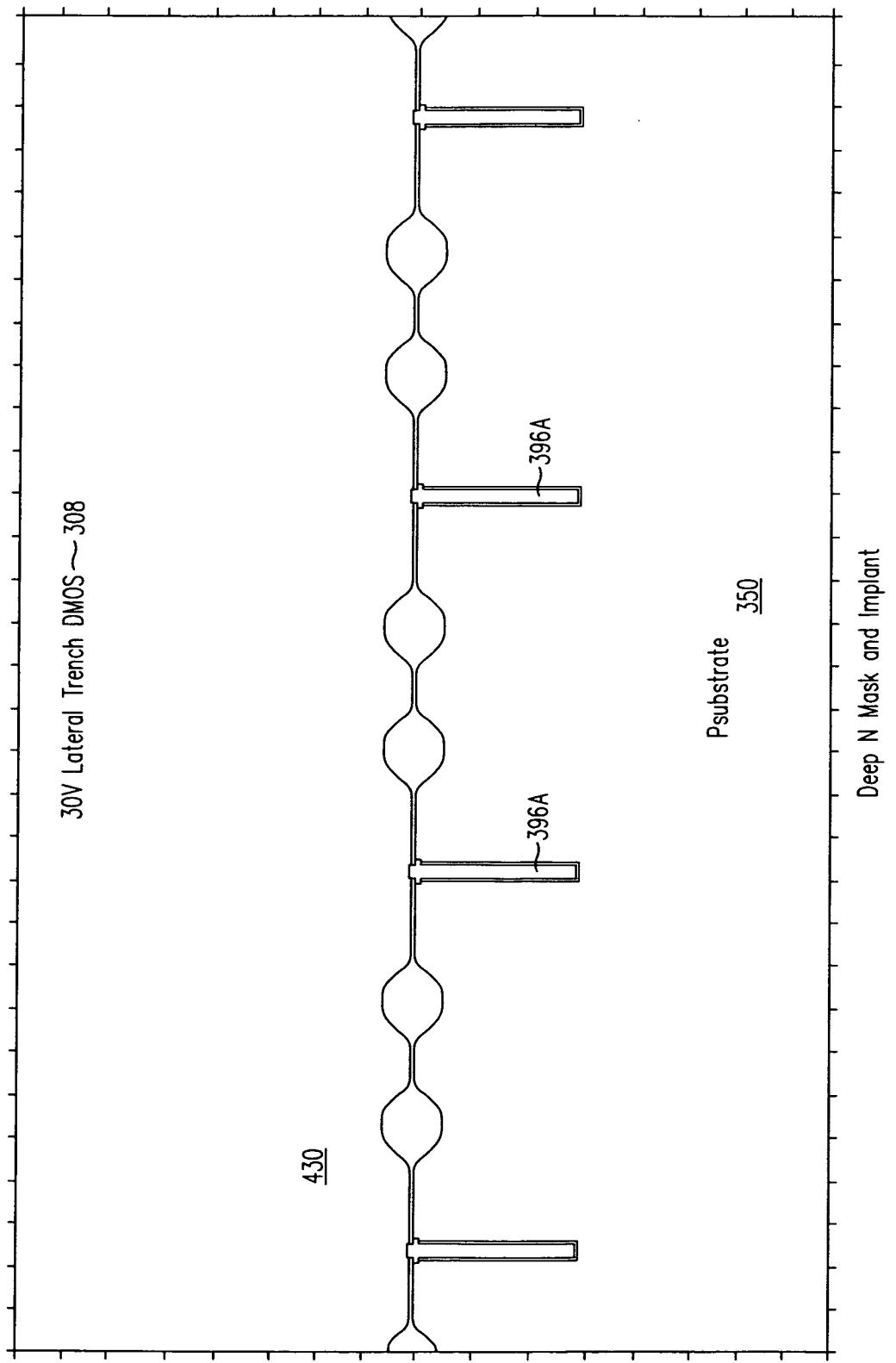
FIG. 35A

Deep N Mask and Implant





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Deep N Mask and Implant
FIG. 35D

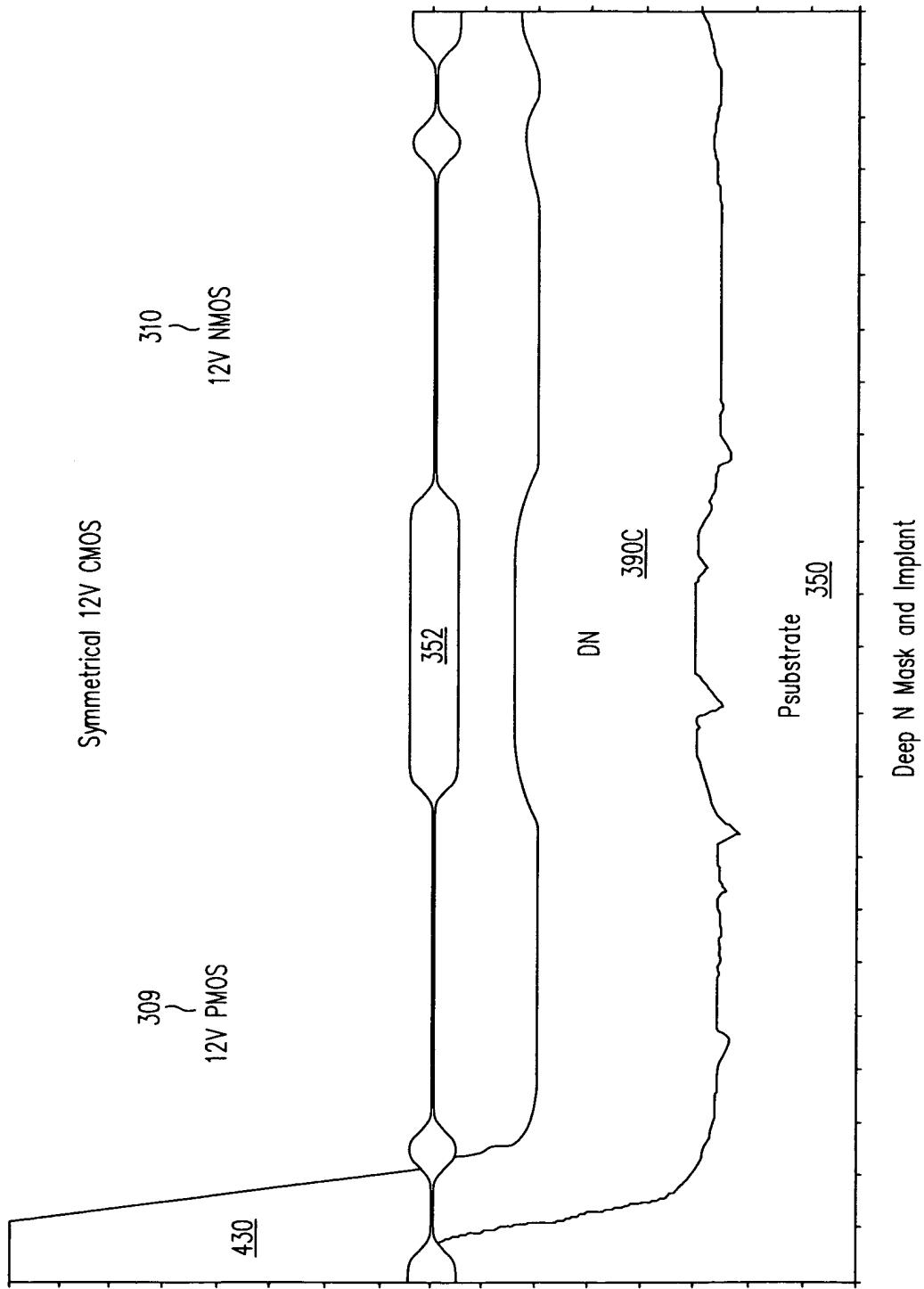


FIG. 35E

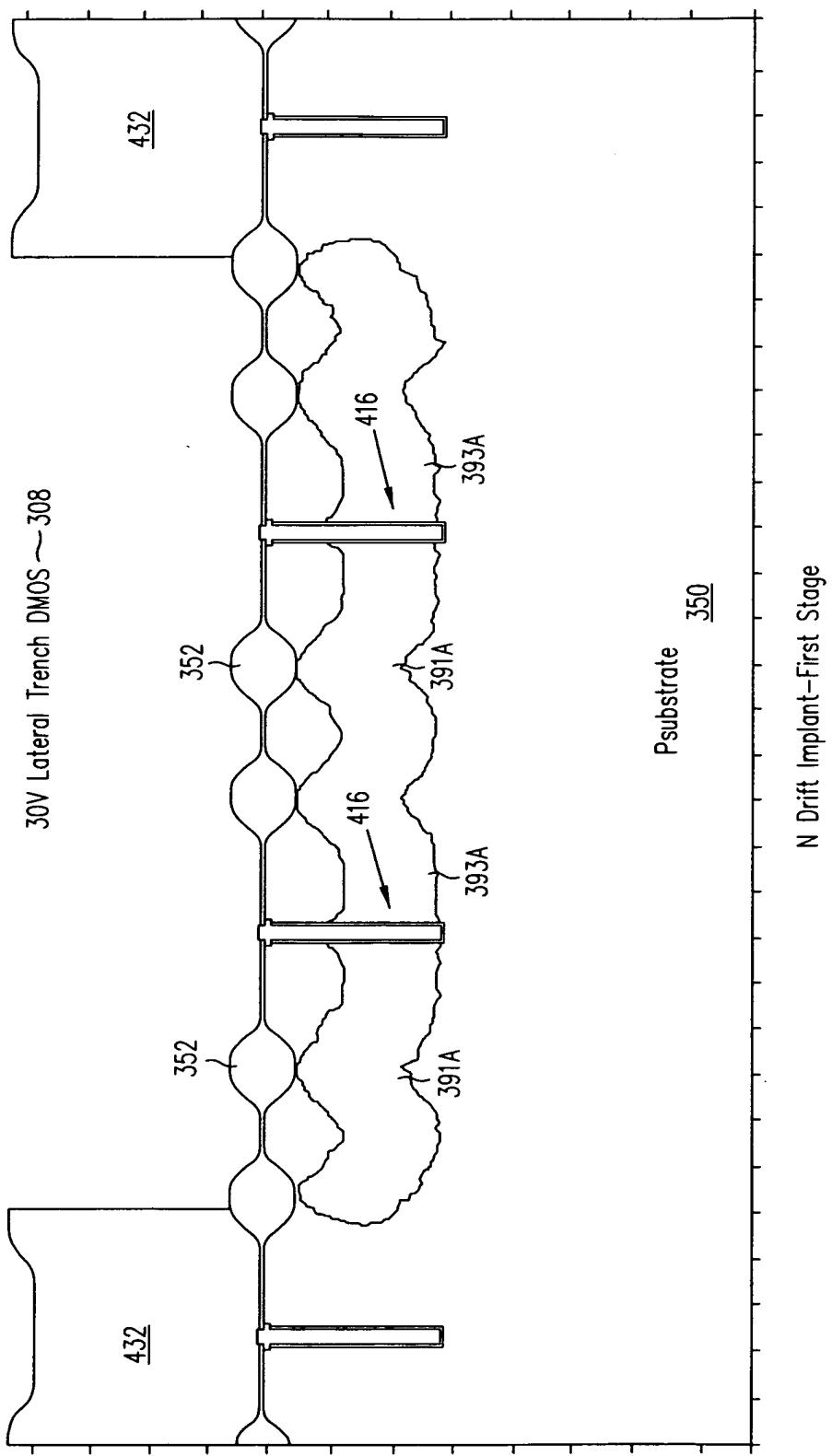


FIG. 36D

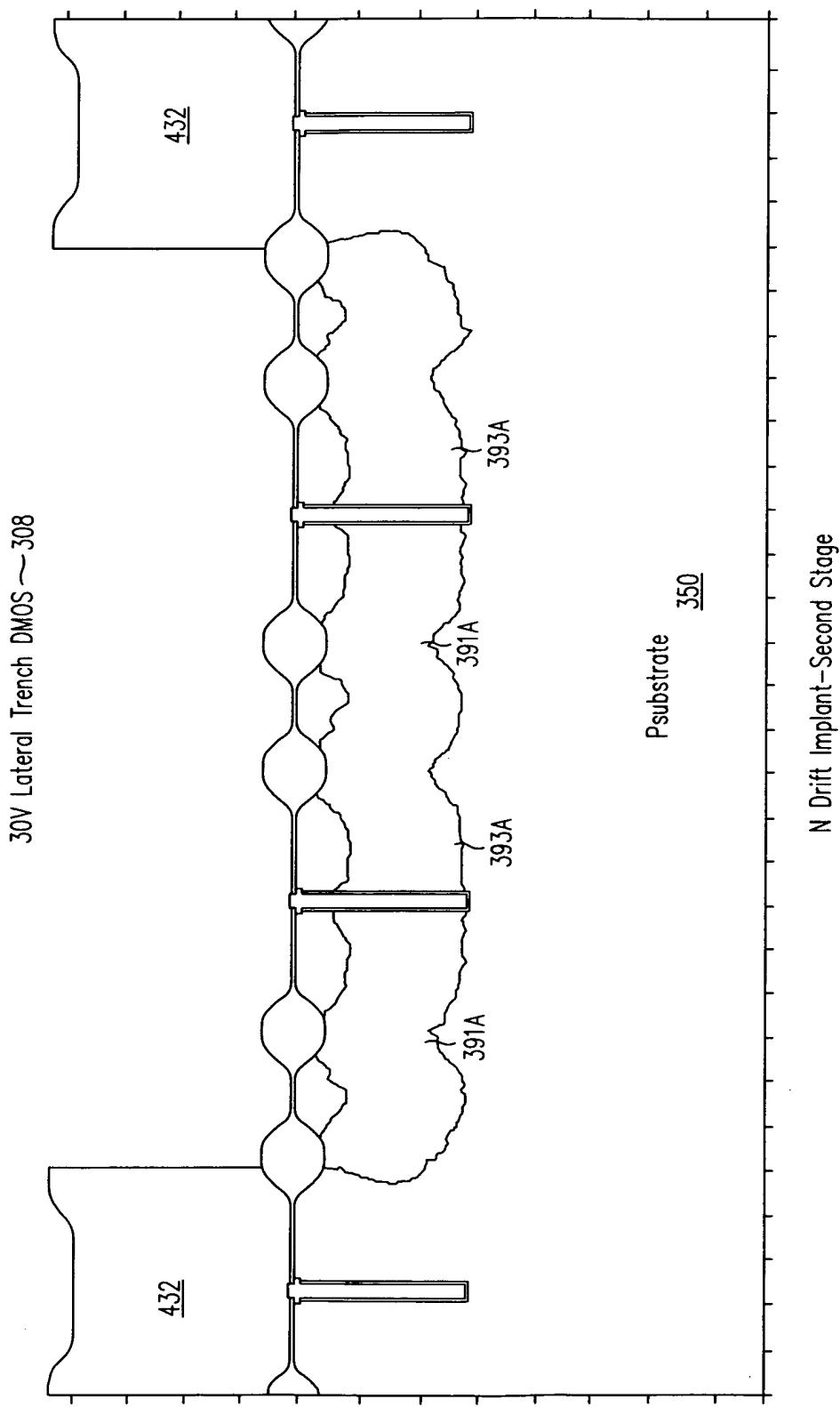


FIG. 37D

N Drift Implant - Second Stage

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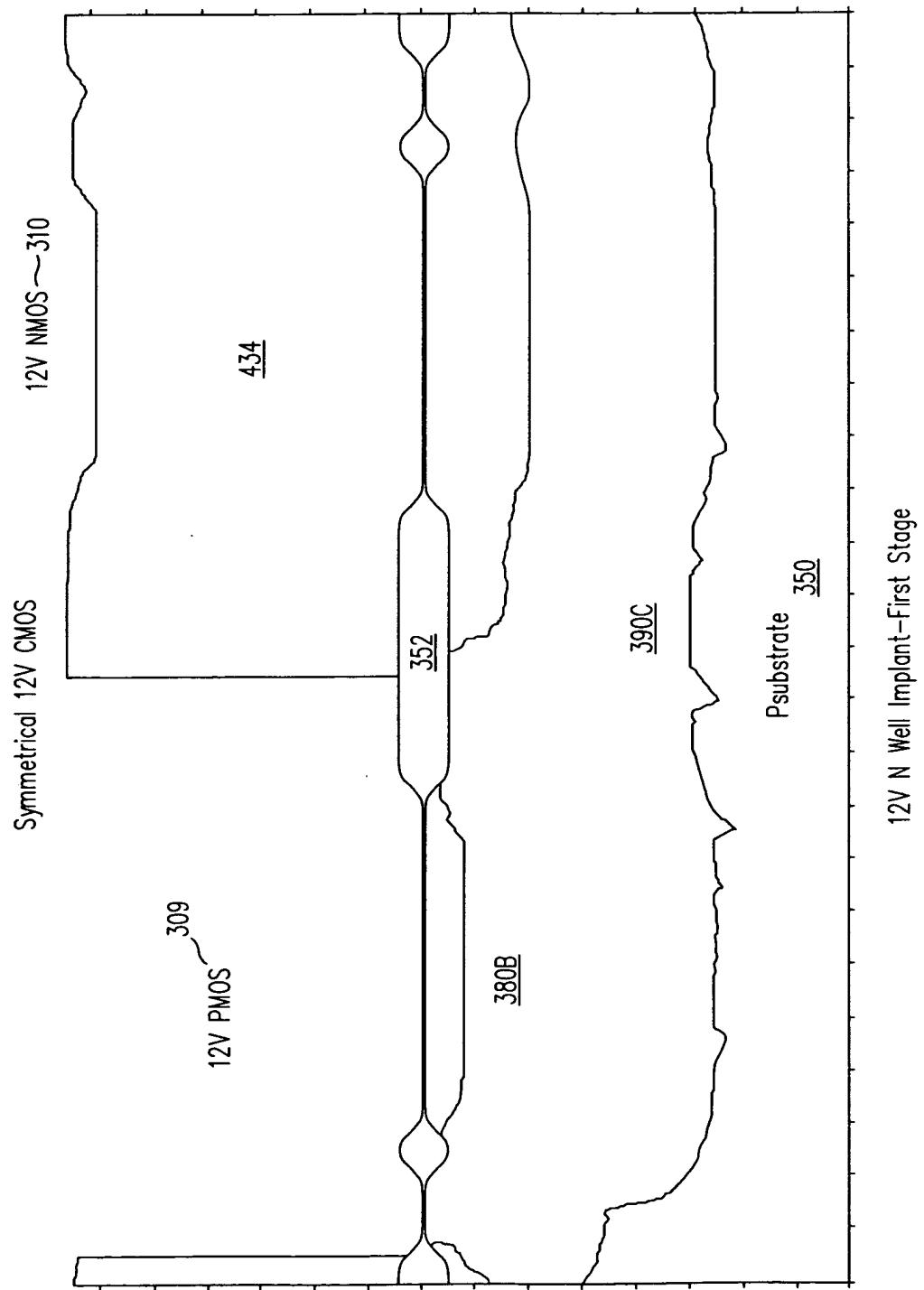
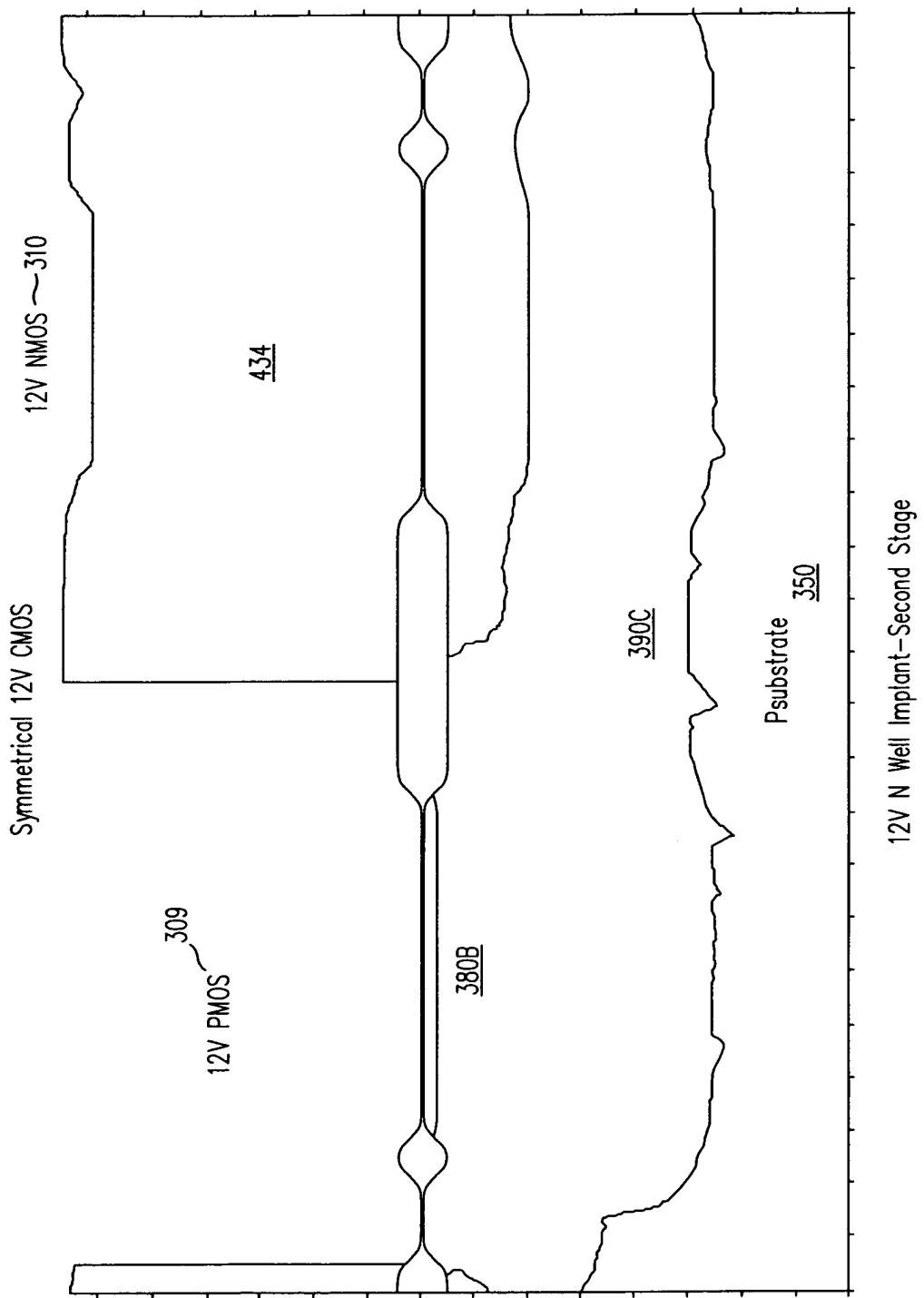


FIG. 38E

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12V N Well Implant - Second Stage

FIG. 39E

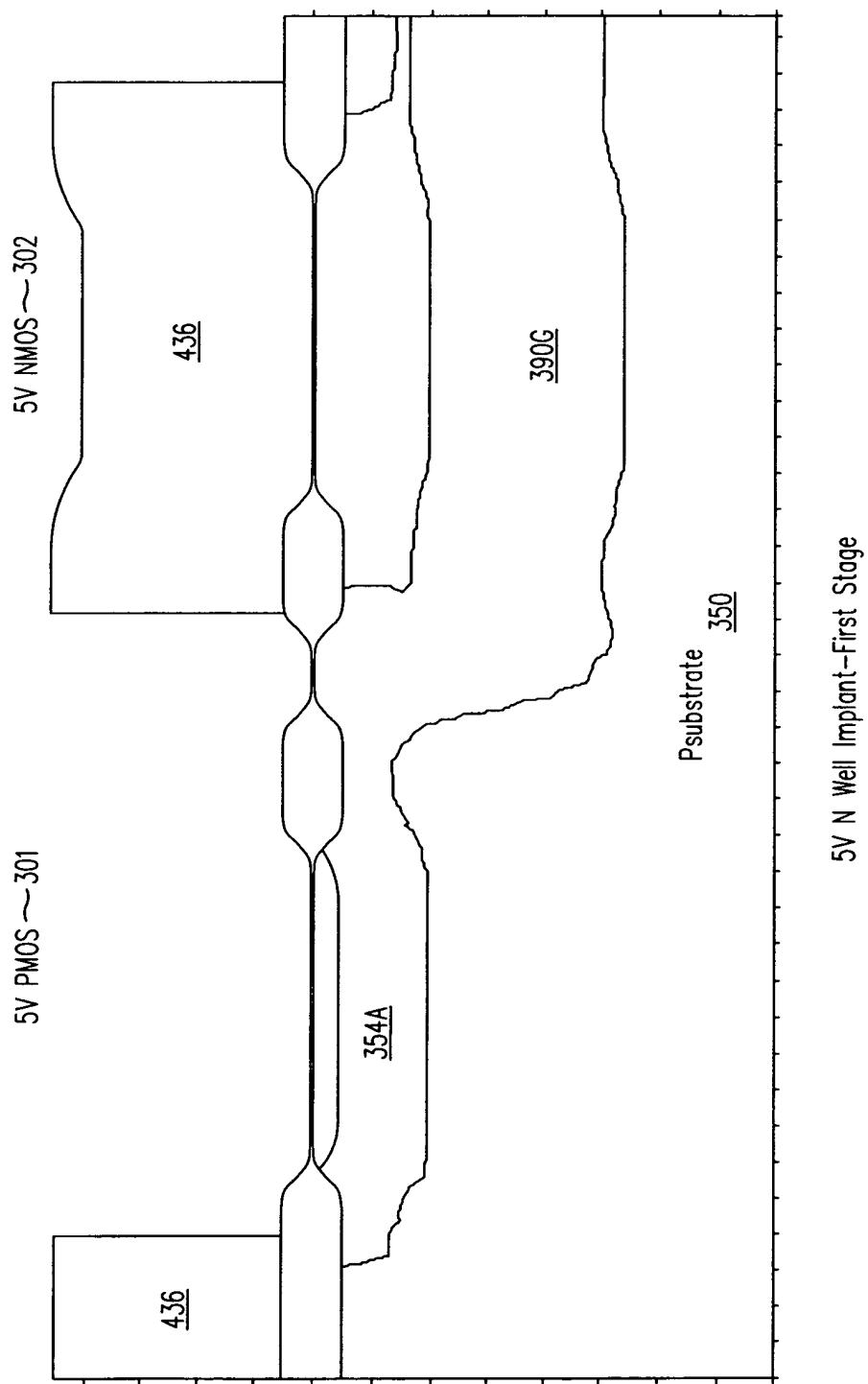


FIG. 40A

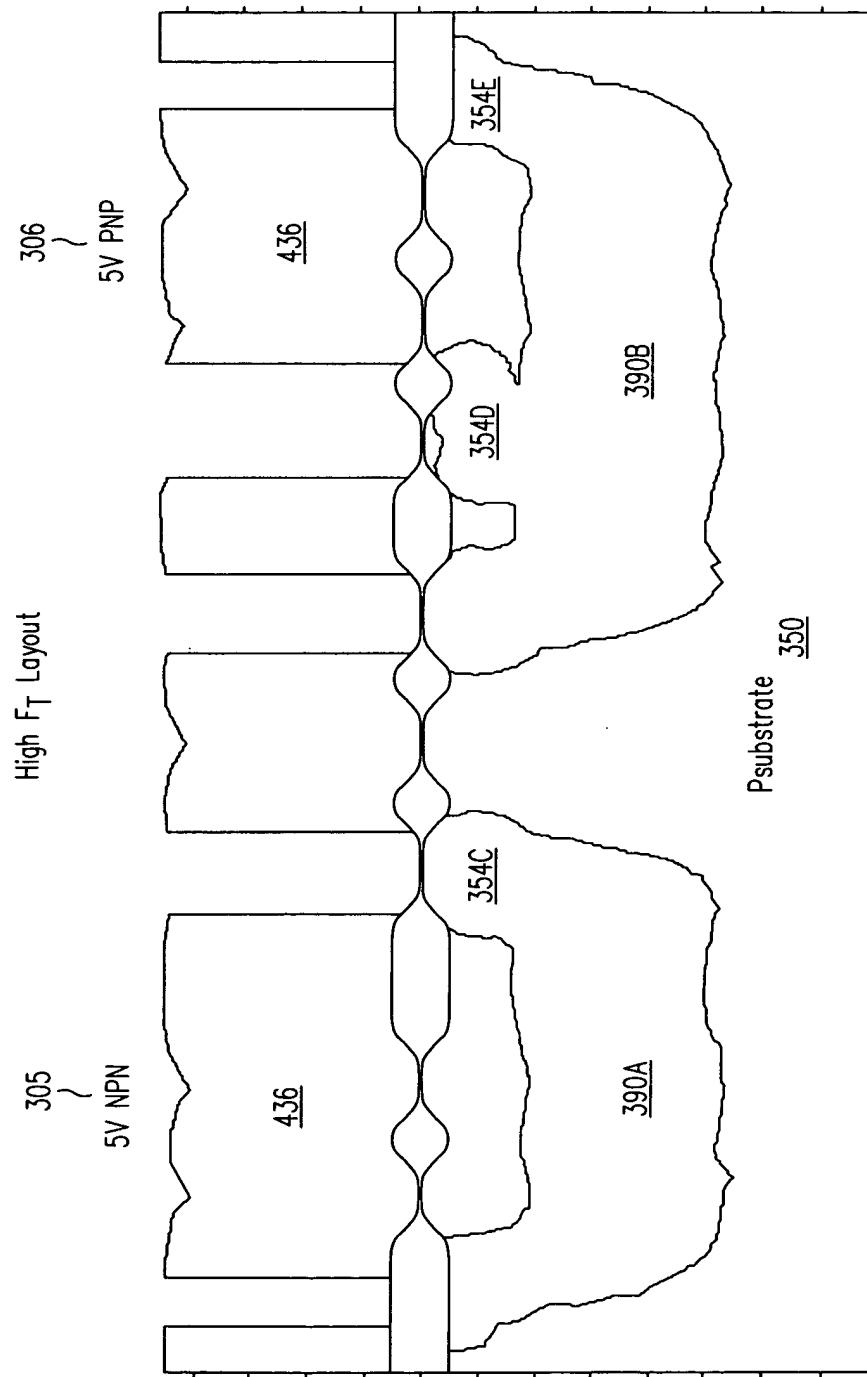


FIG. 40B

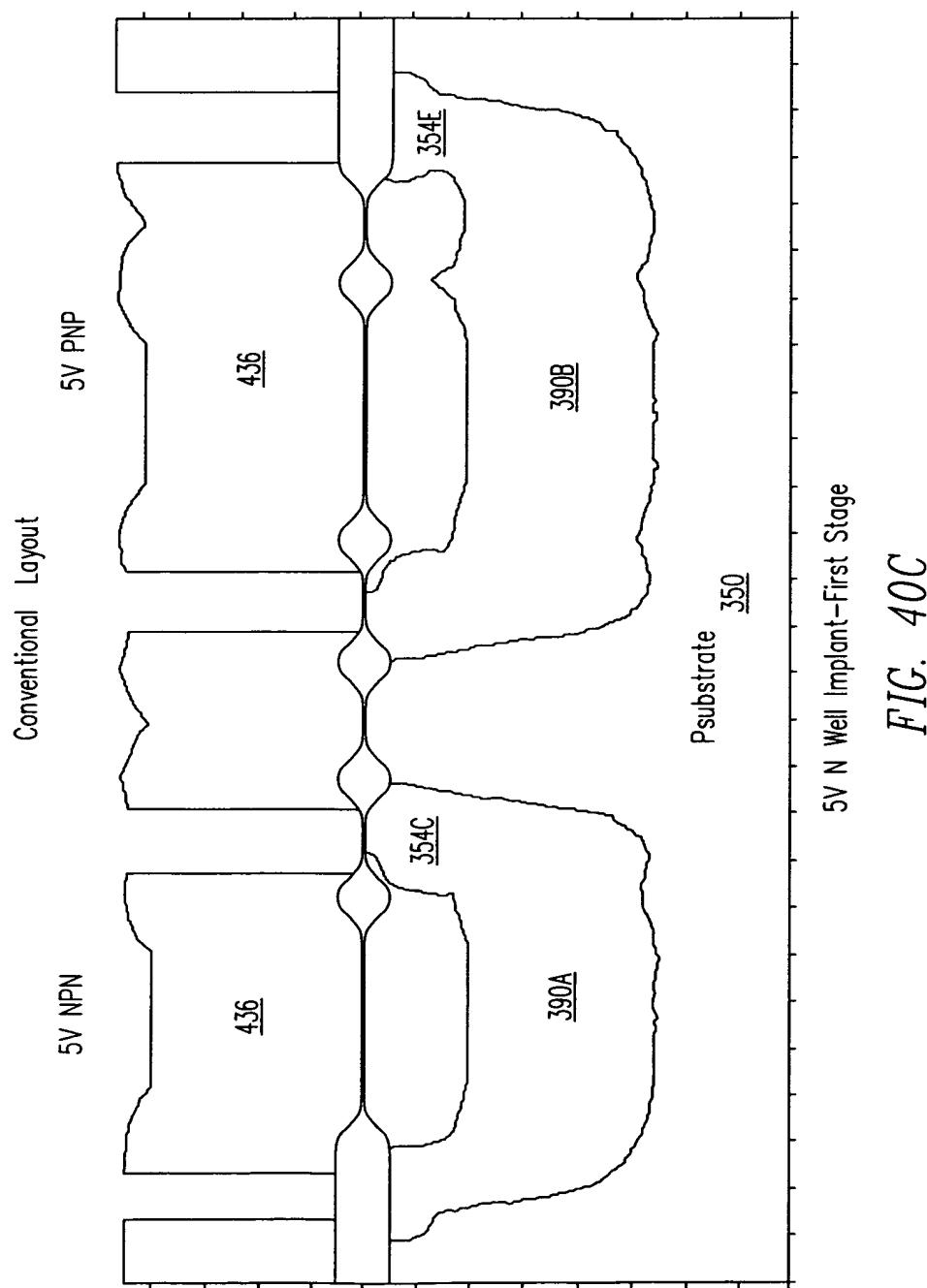


FIG. 40C

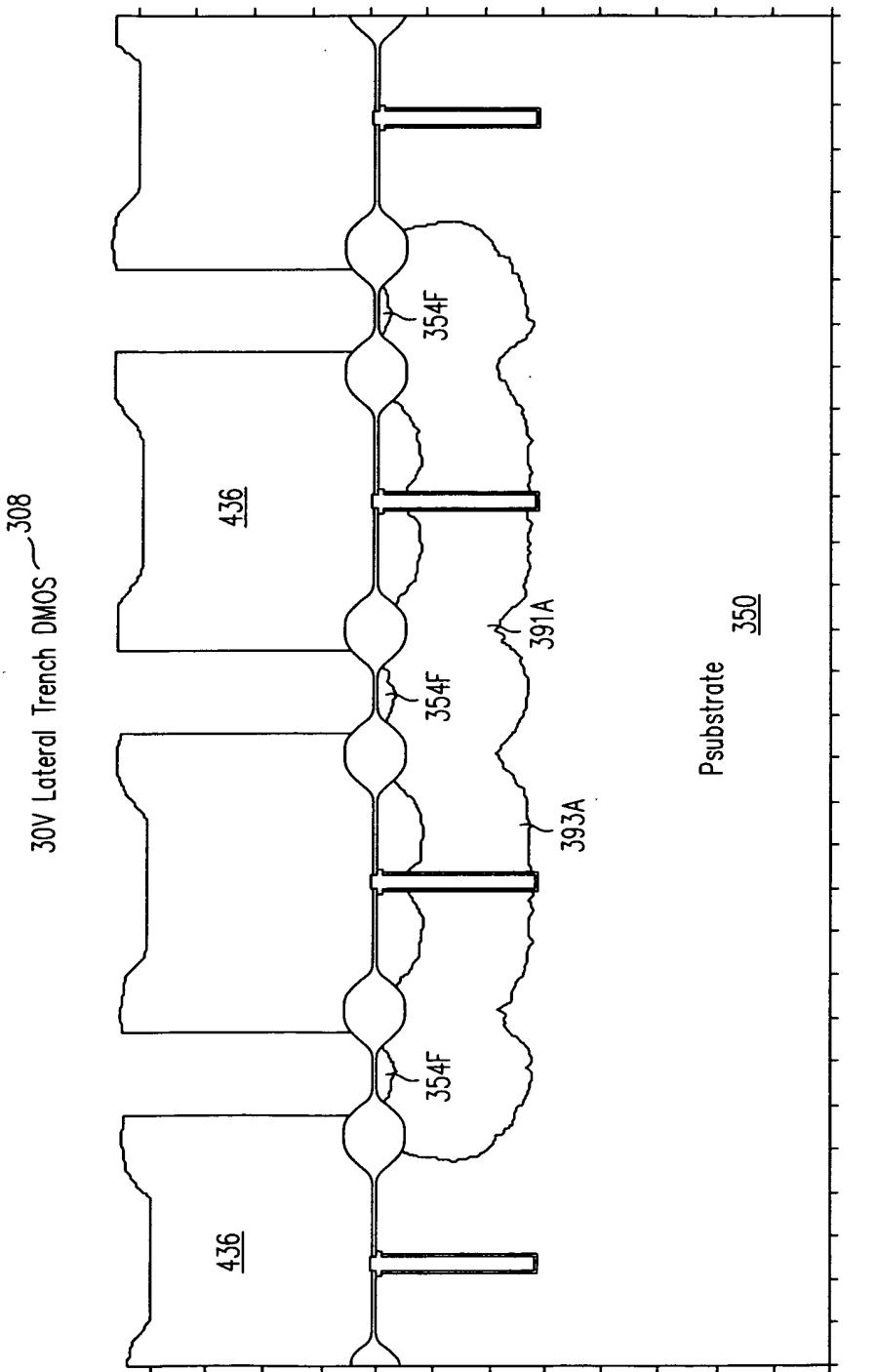
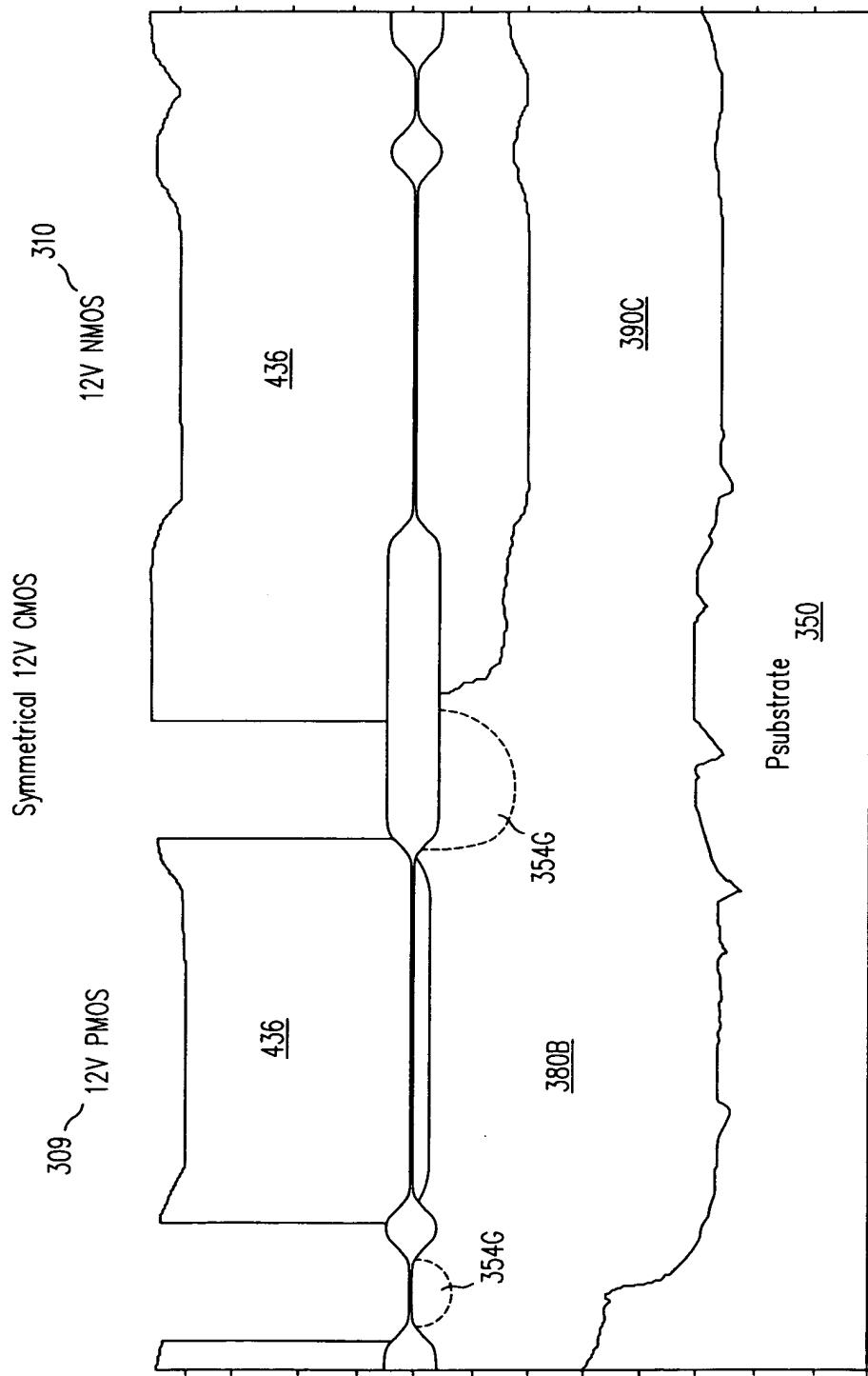


FIG. 40D

5V N Well Implant-First Stage

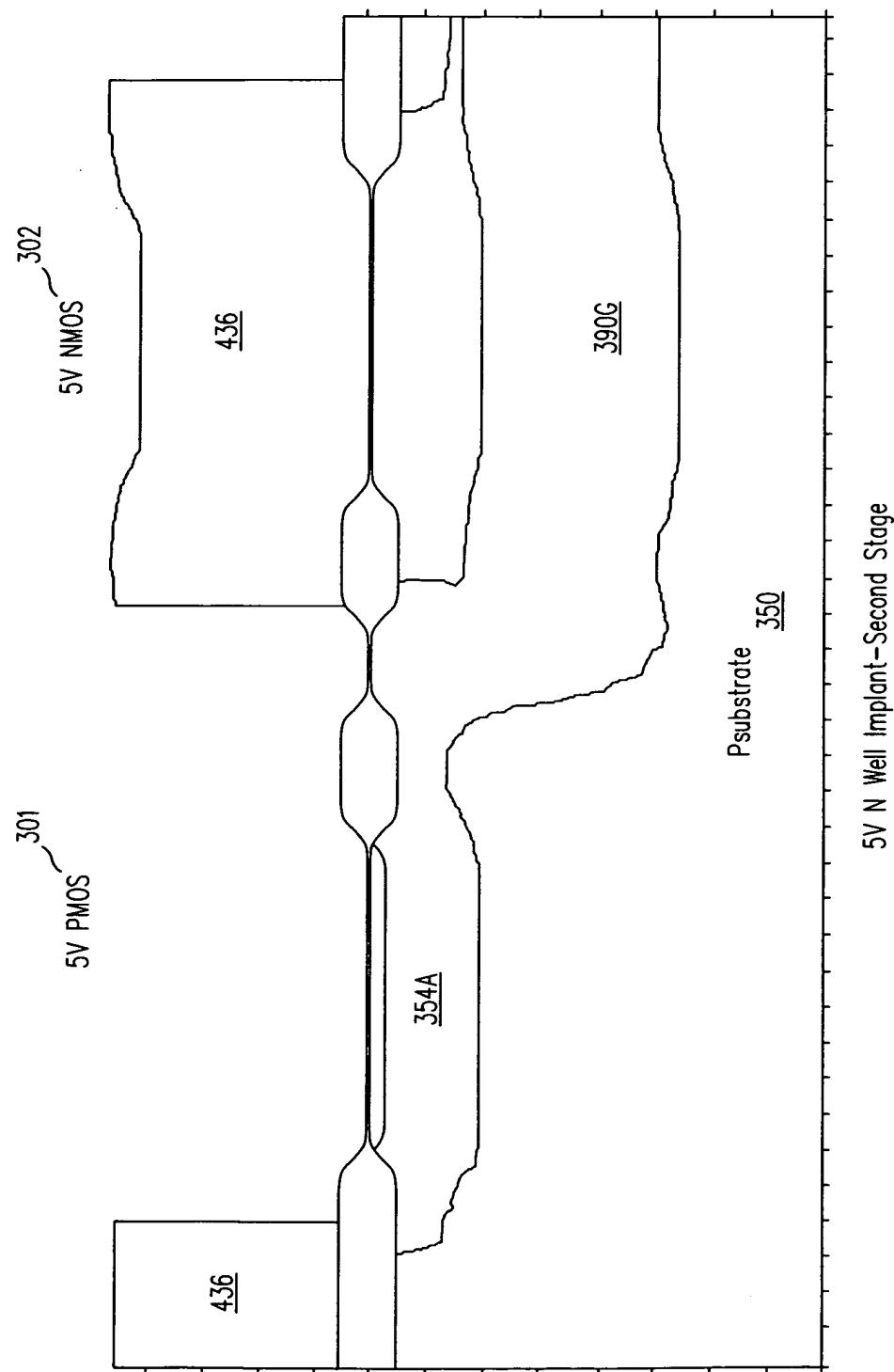
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5V N Well Implant-First Stage

FIG. 40E

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5V N Well Implant-Second Stage

FIG. 41A

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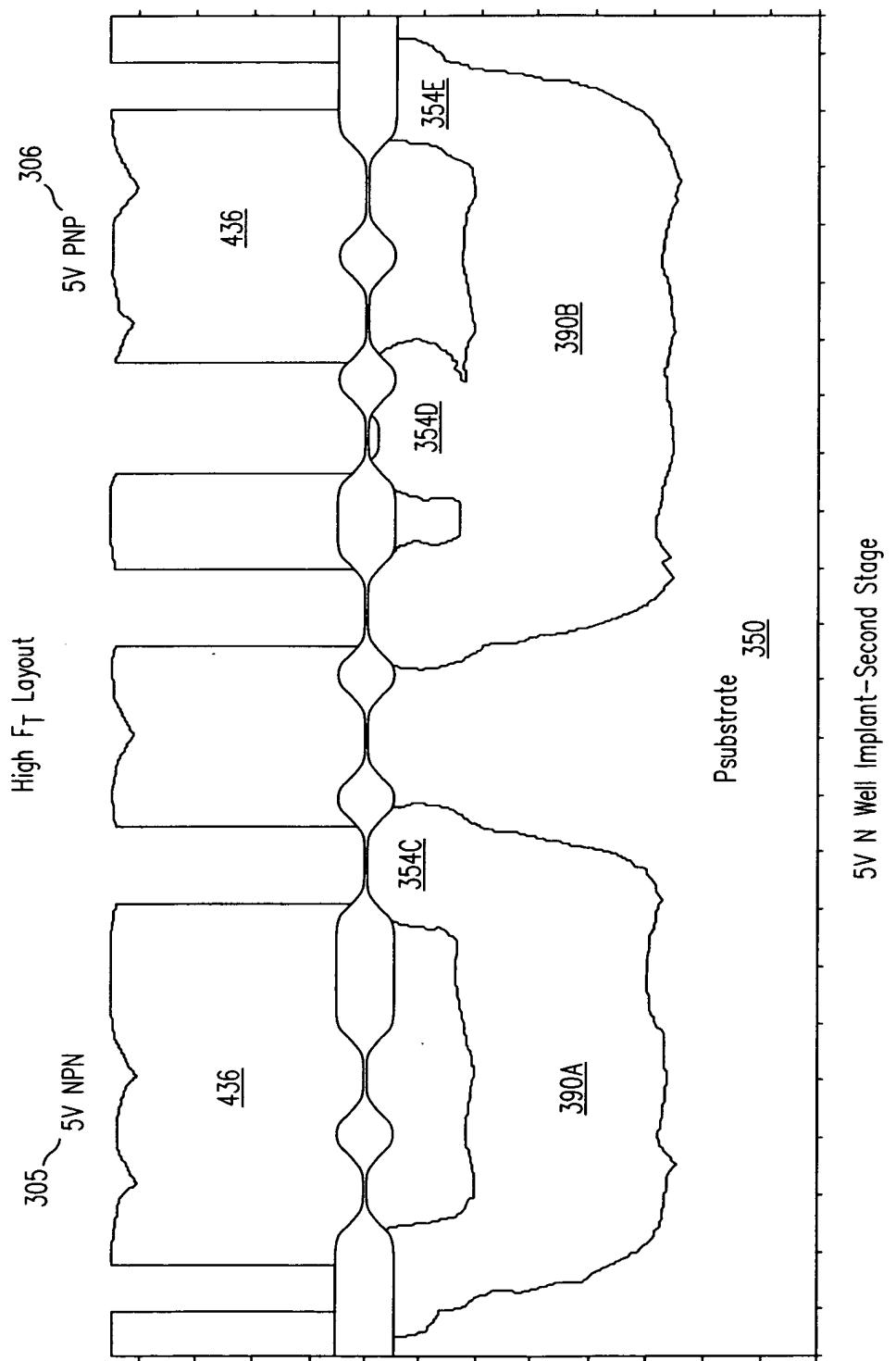


FIG. 41B

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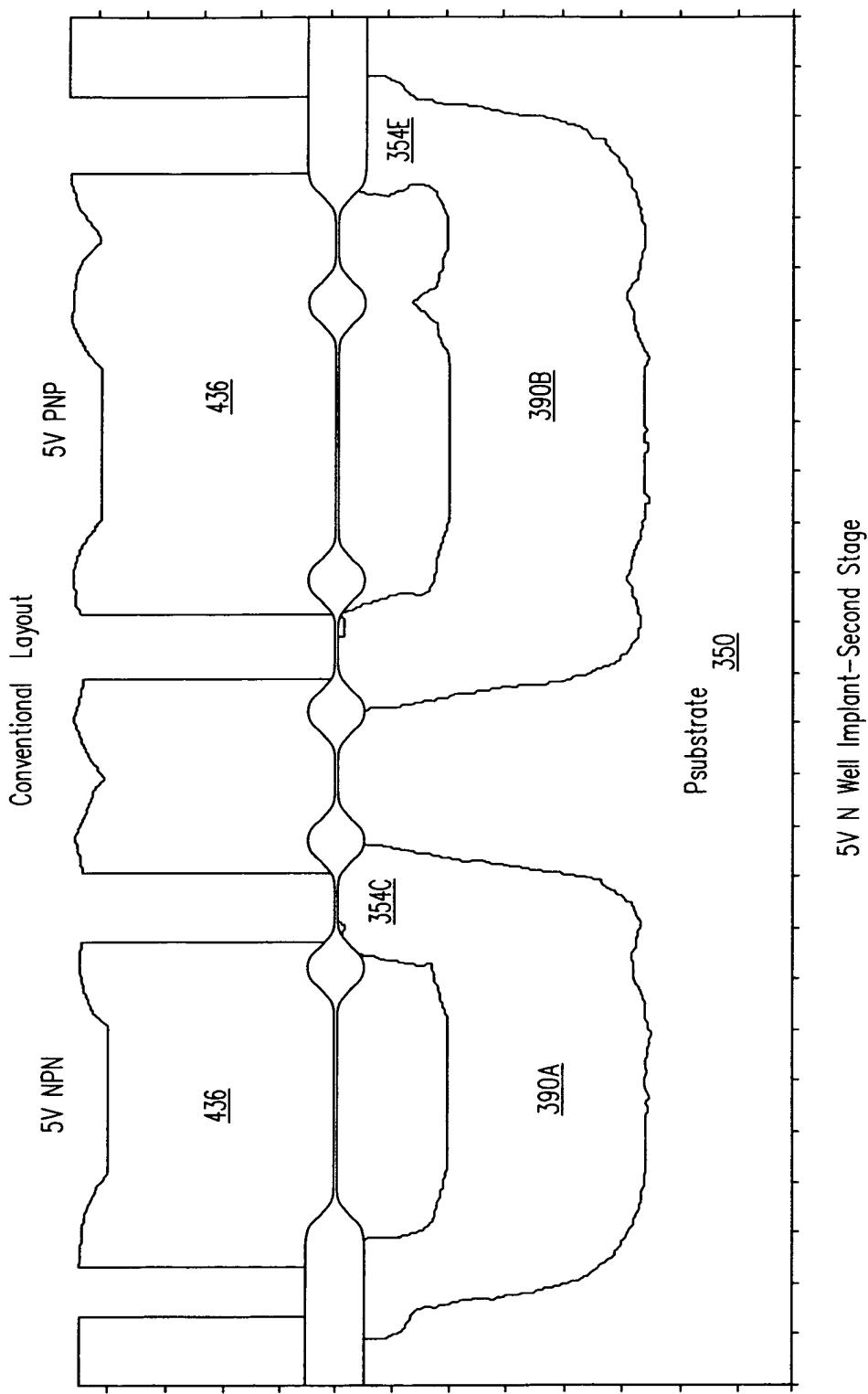


FIG. 41C

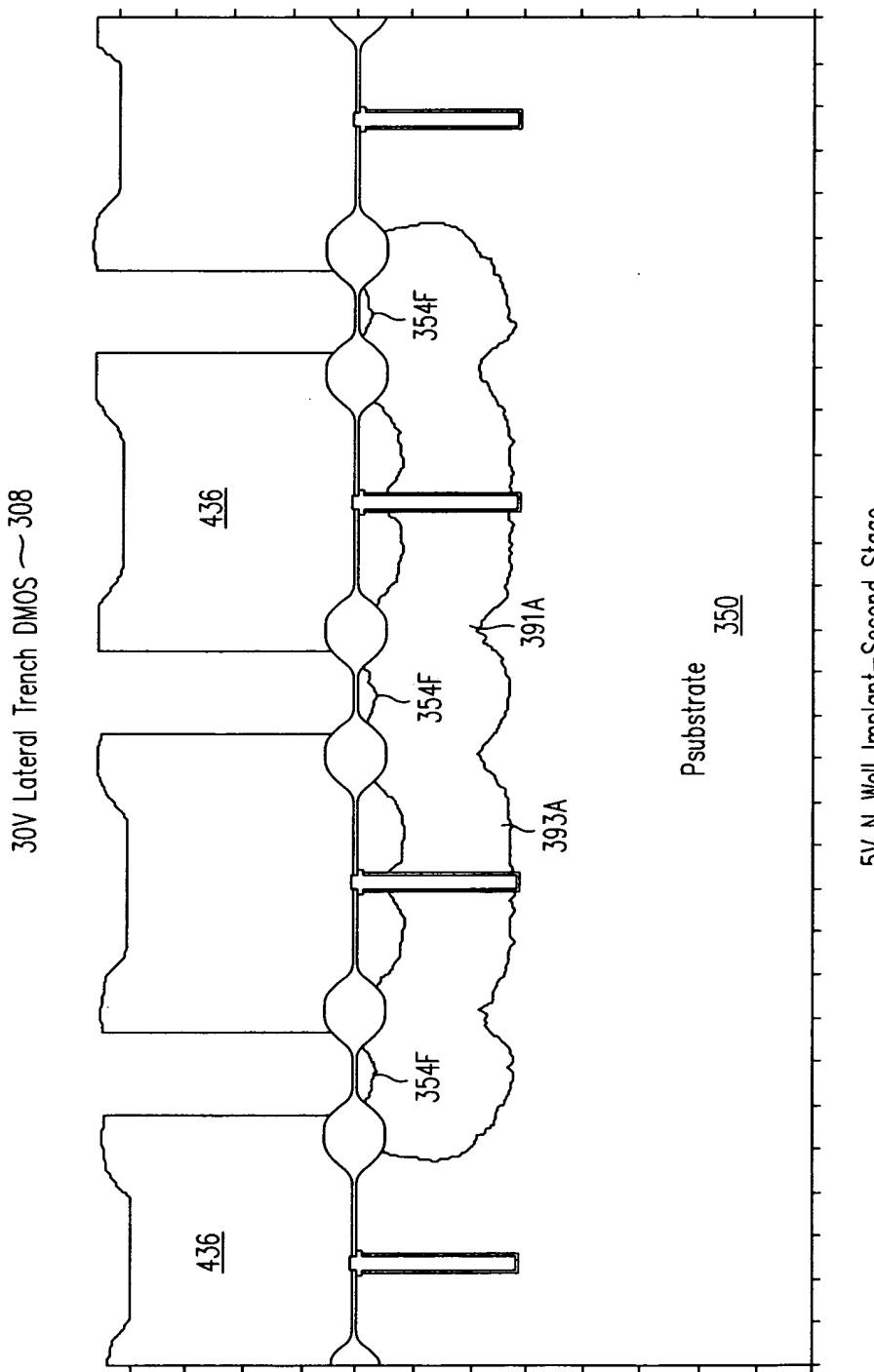
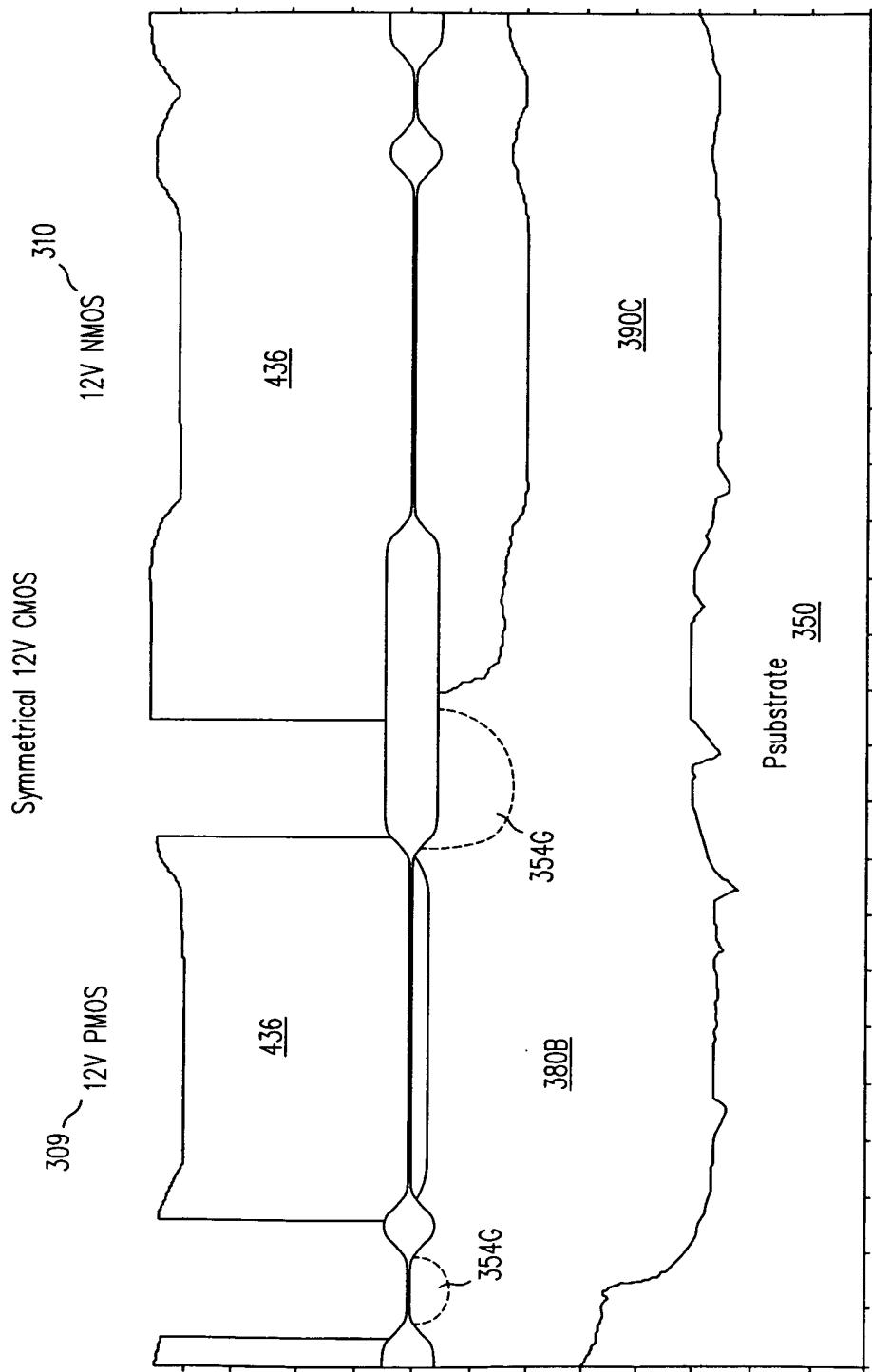


FIG. 41D

5V N Well Implant—Second Stage

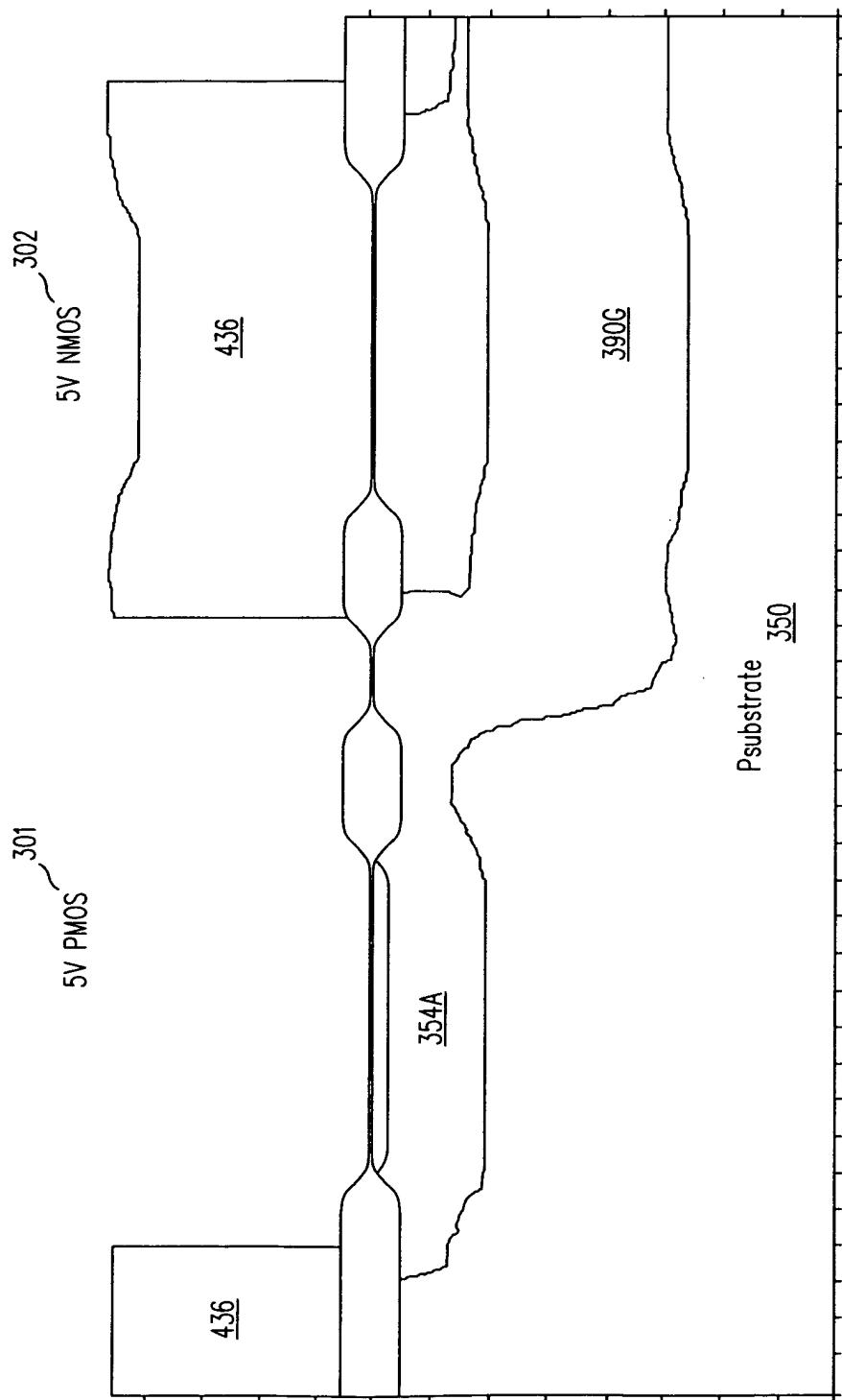
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5V N Well Implant—Second Stage

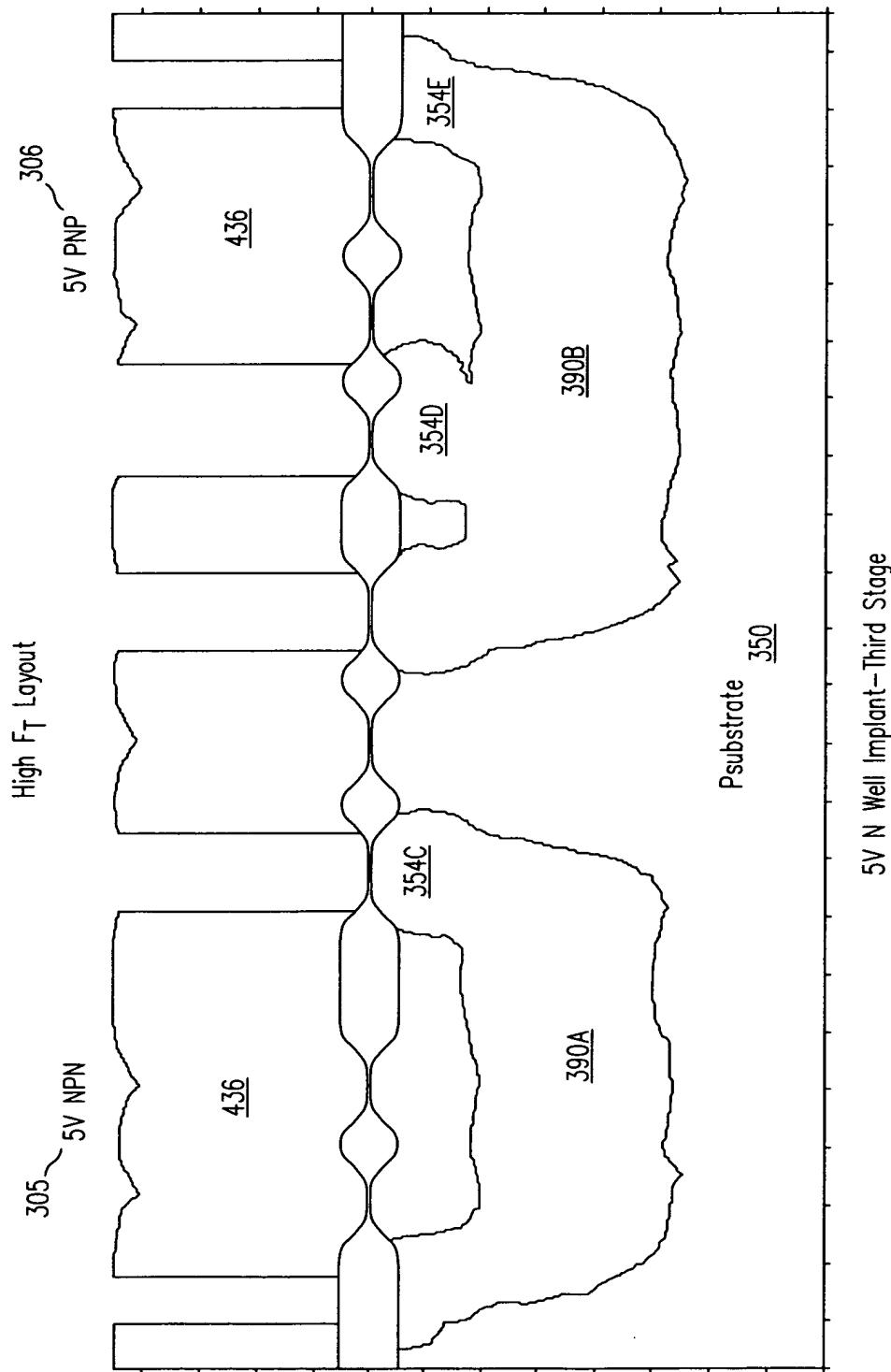
FIG. 41E

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5V N Well Implant- Third Stage

FIG. 42A



5V N Well Implant- Third Stage

FIG. 42B

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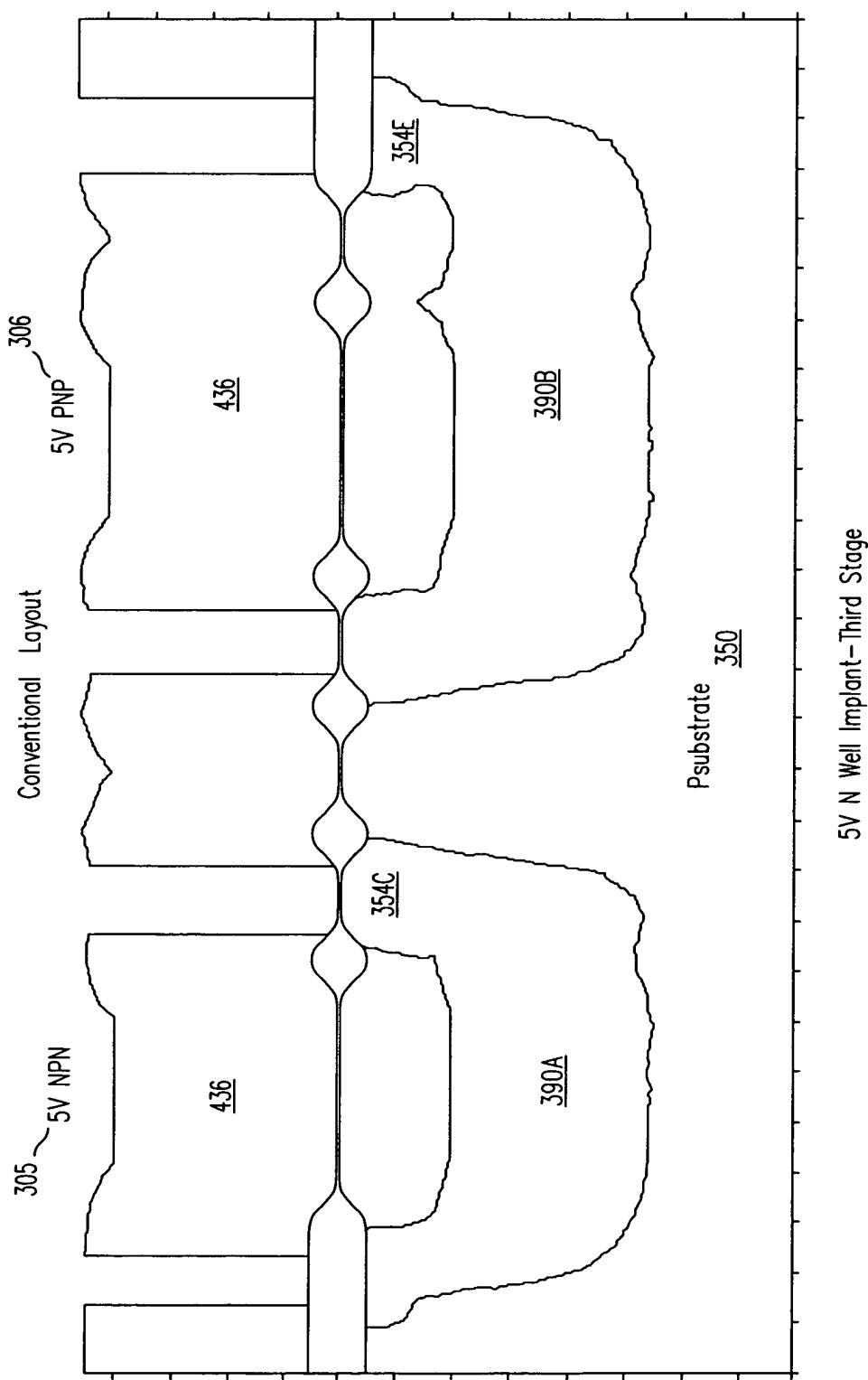


FIG. 42C

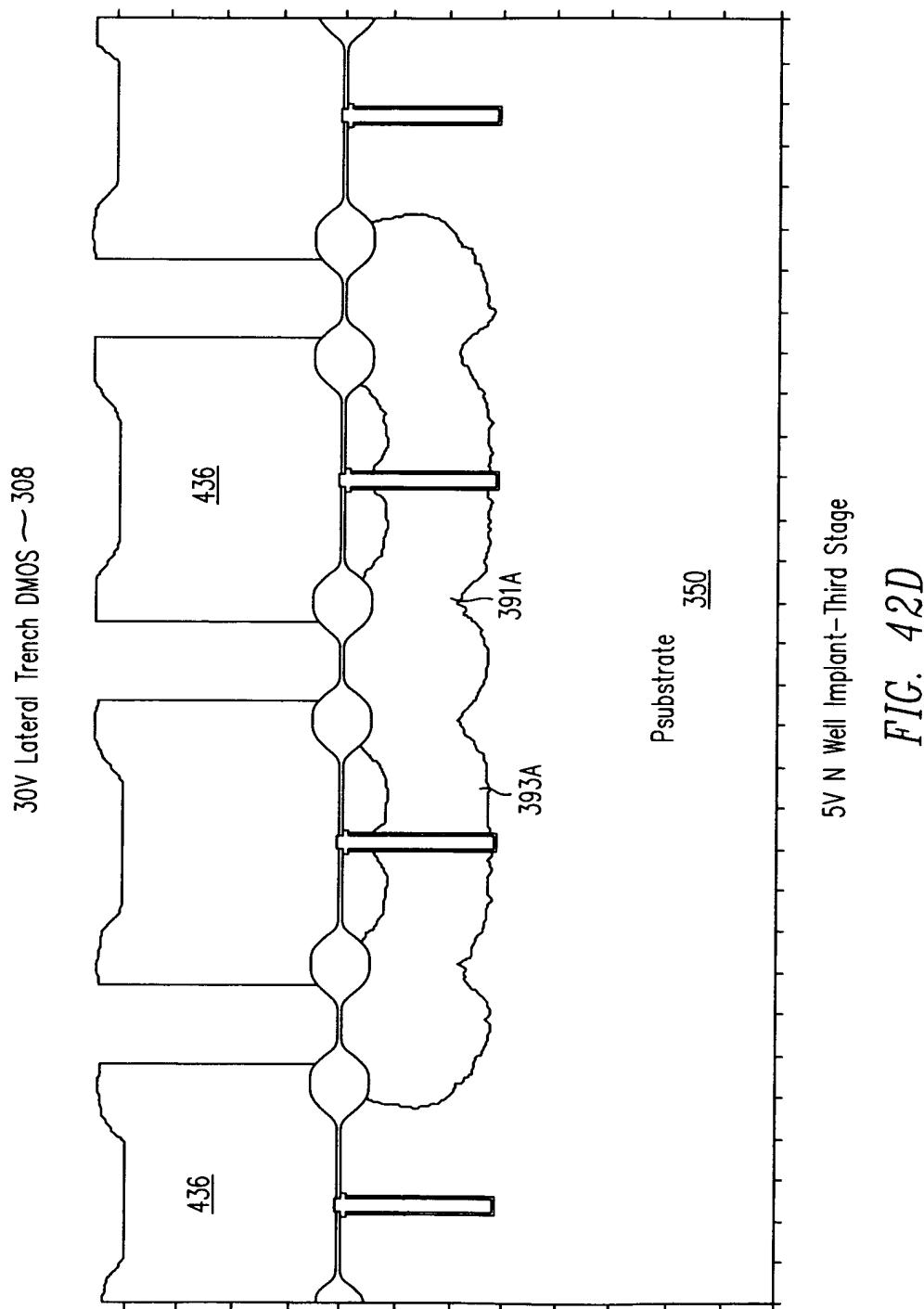
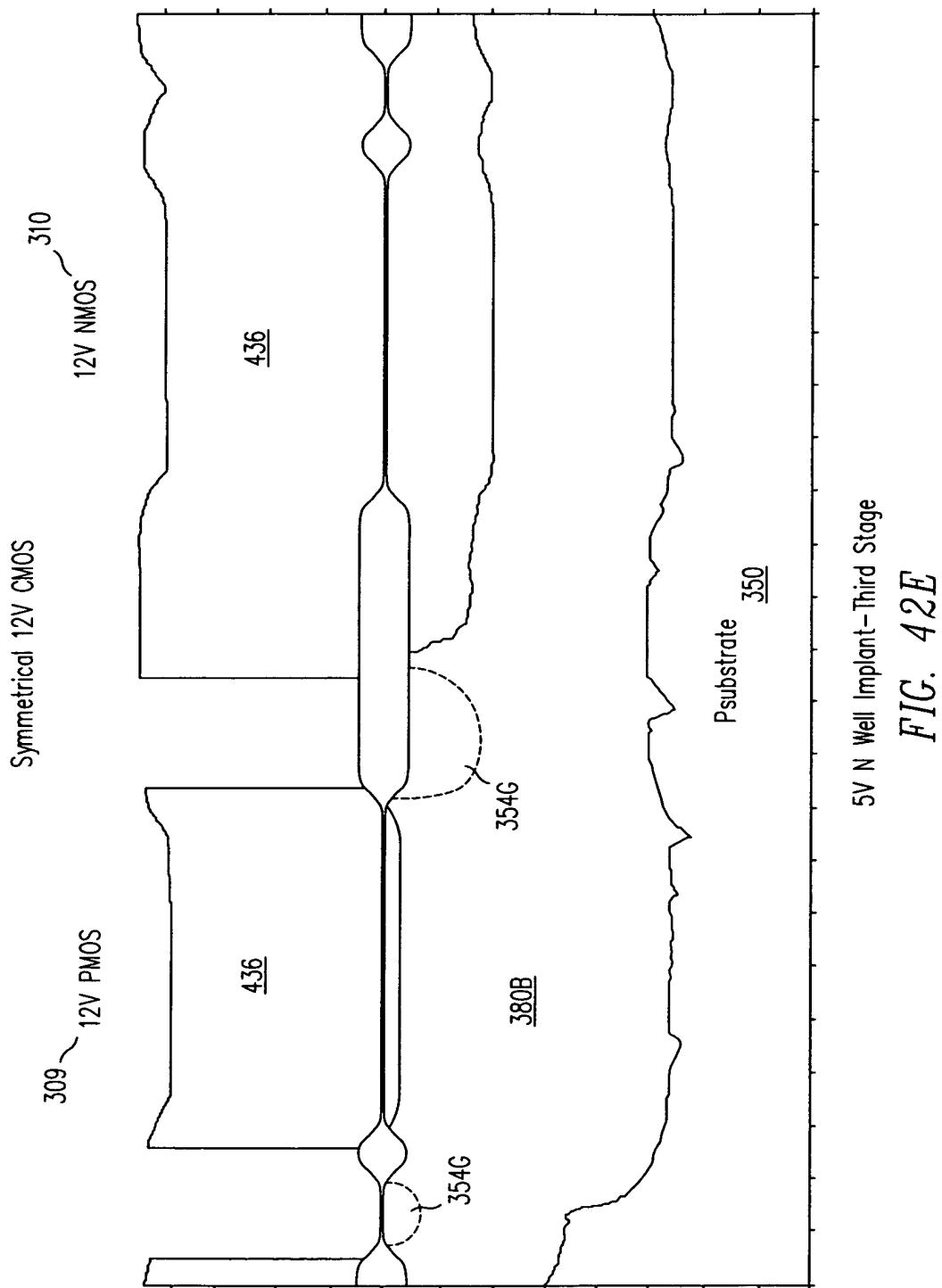
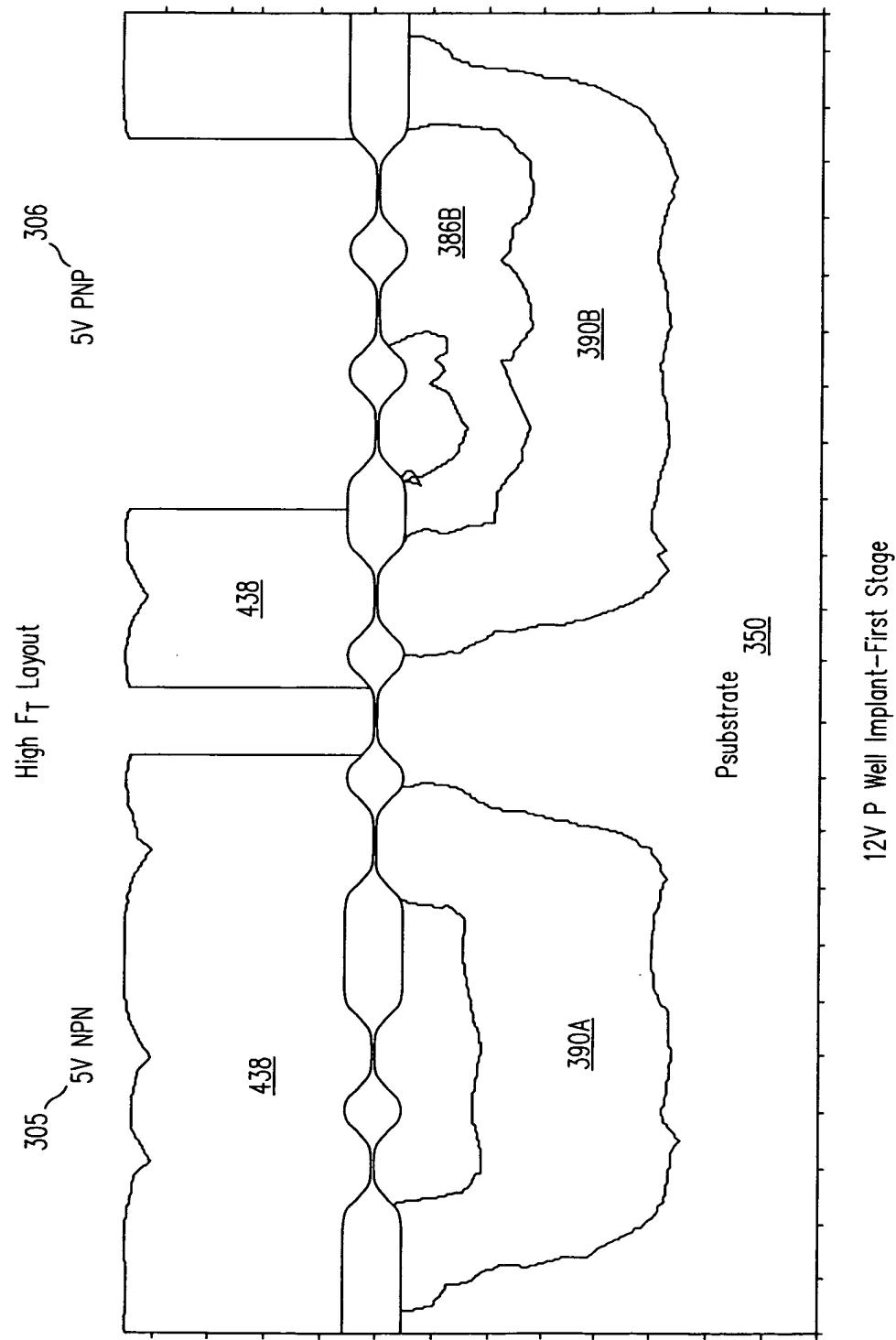


FIG. 42D





12V P Well Implant—First Stage

FIG. 43B

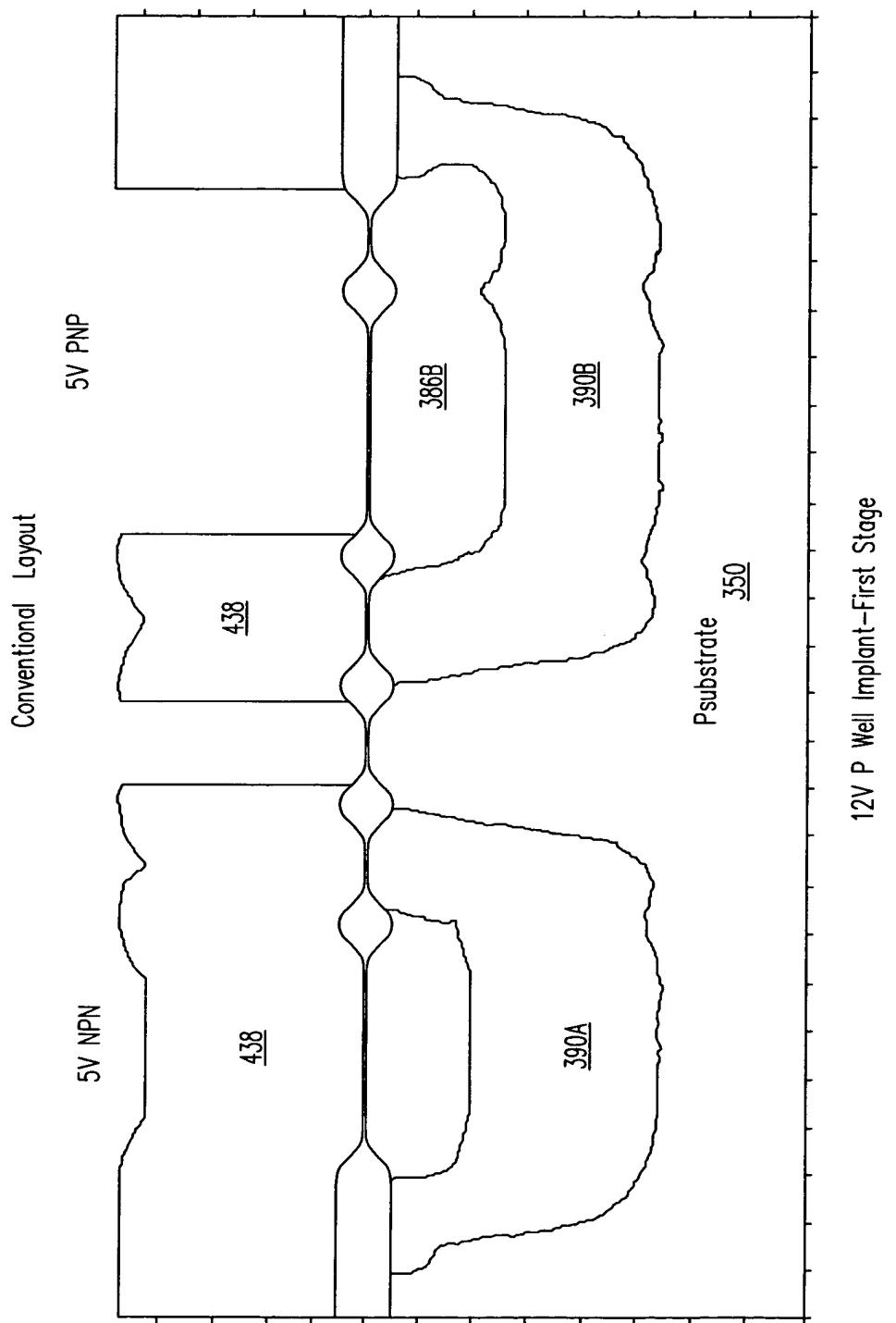
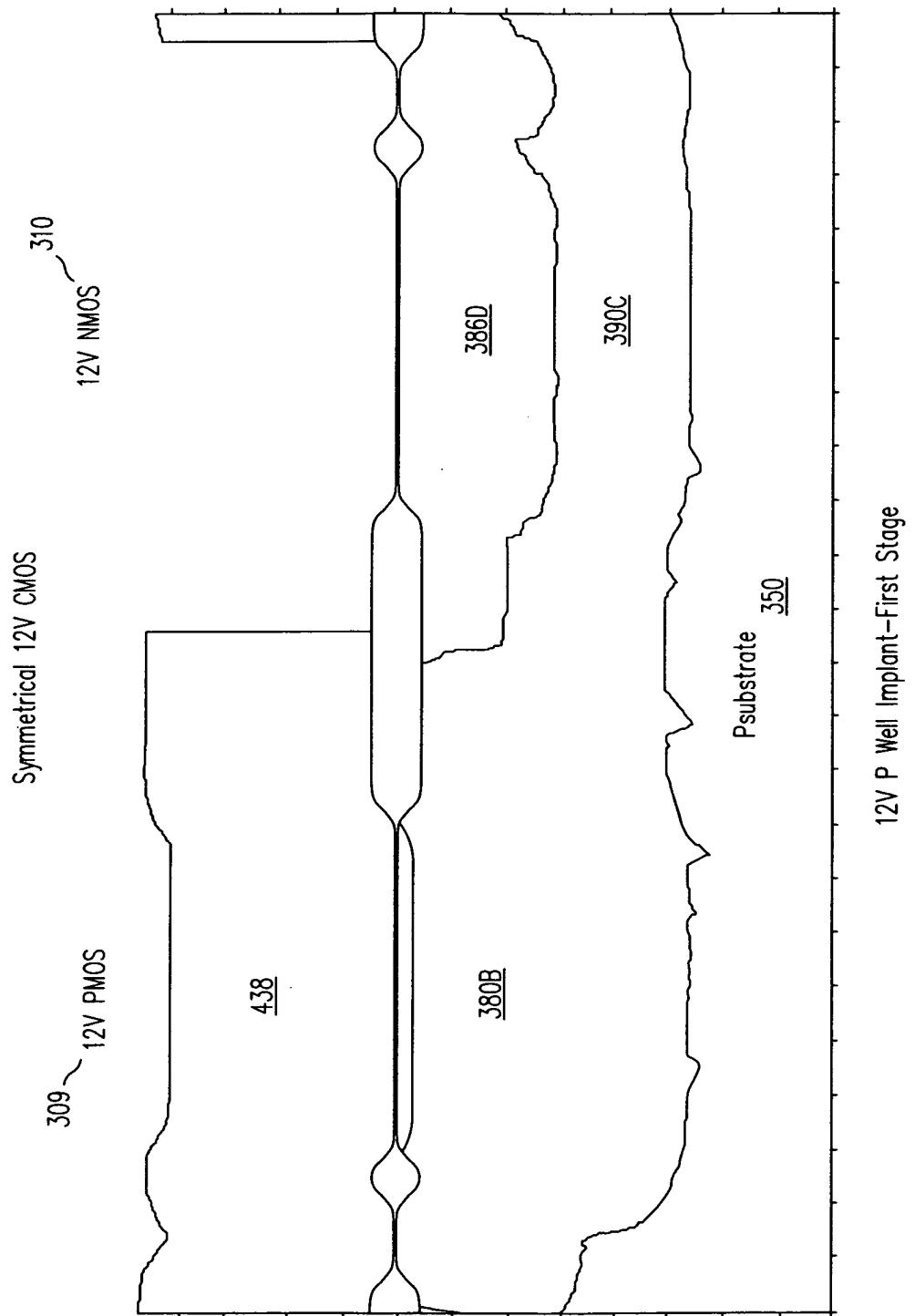


FIG. 43C



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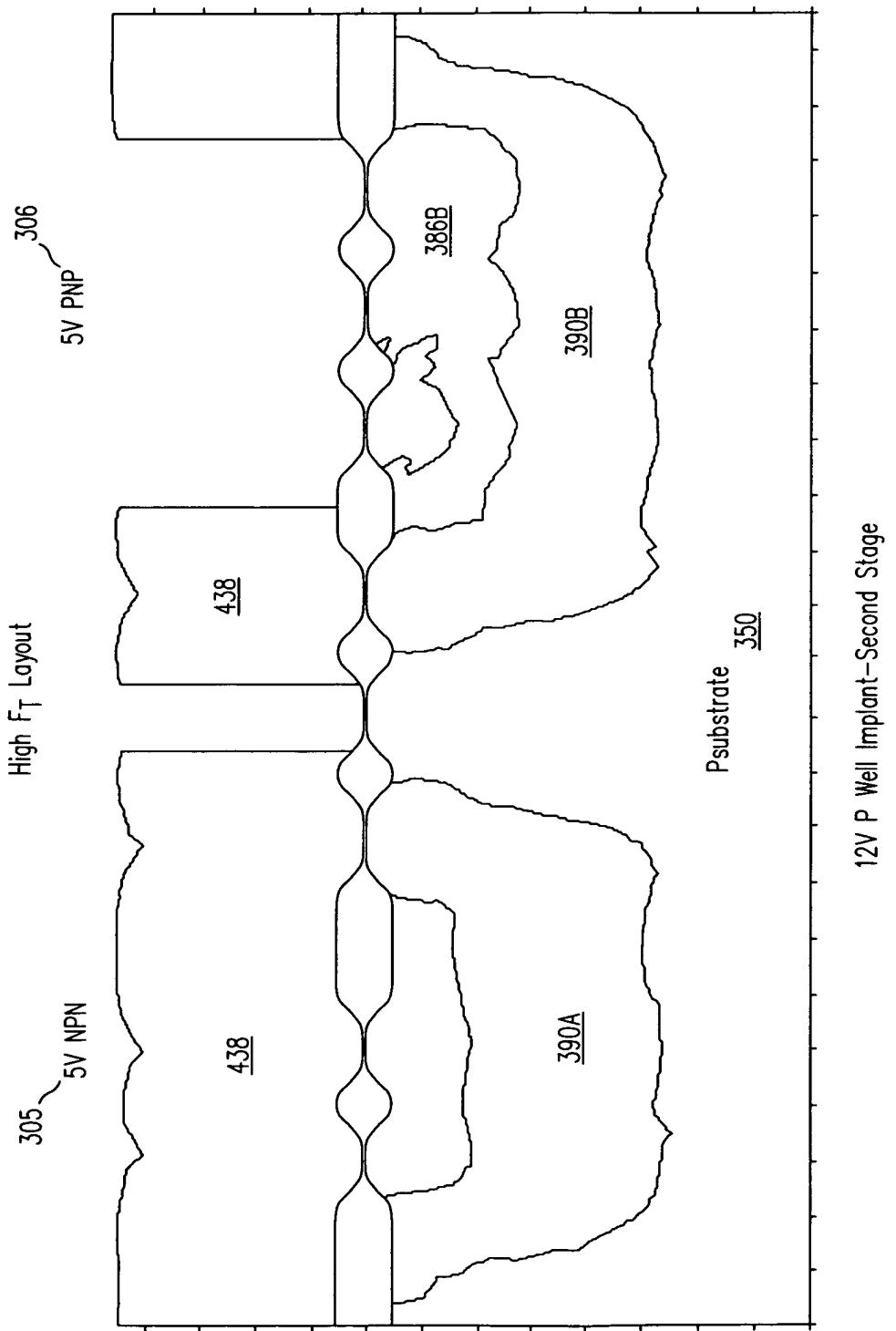


FIG. 44B

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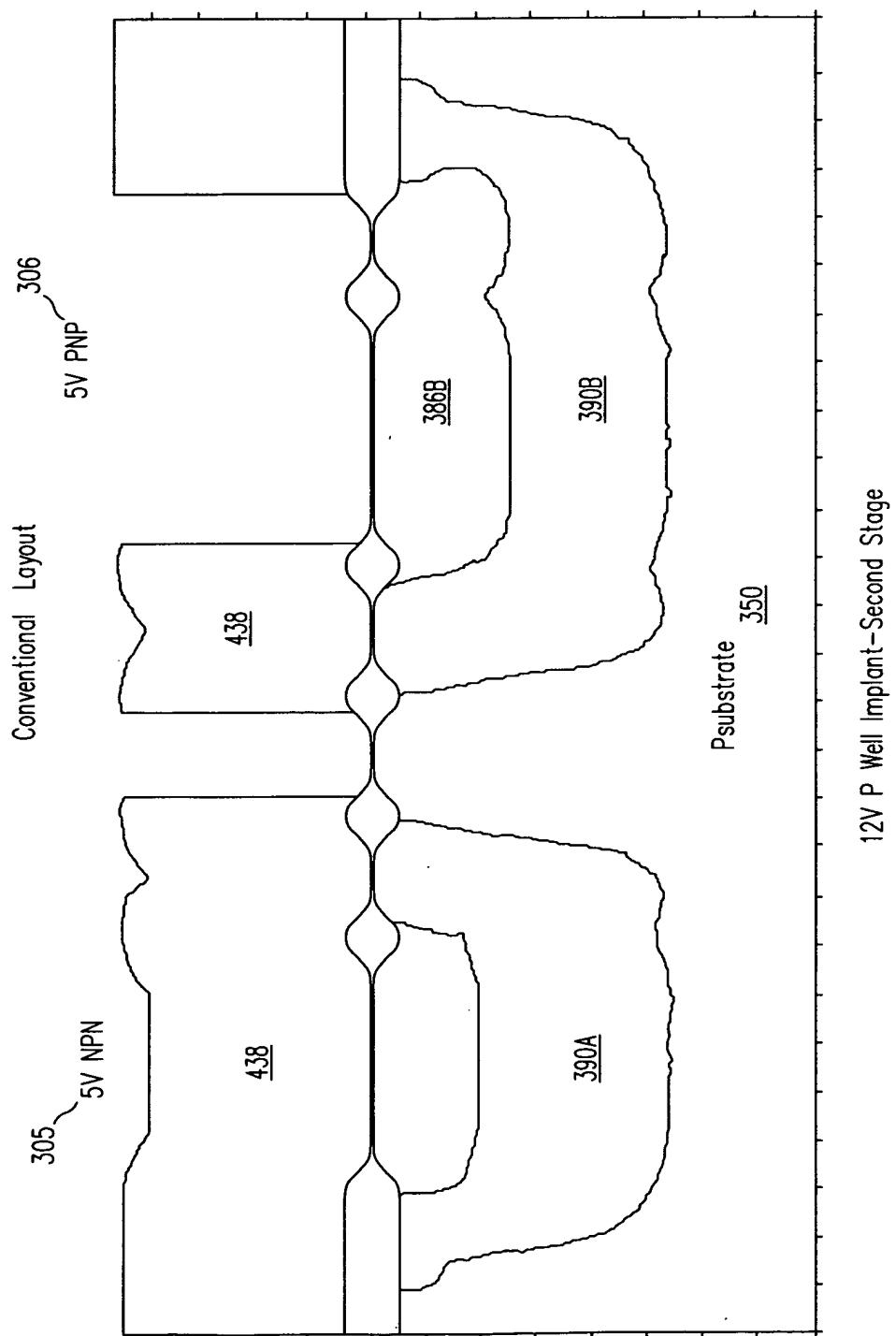


FIG. 44C

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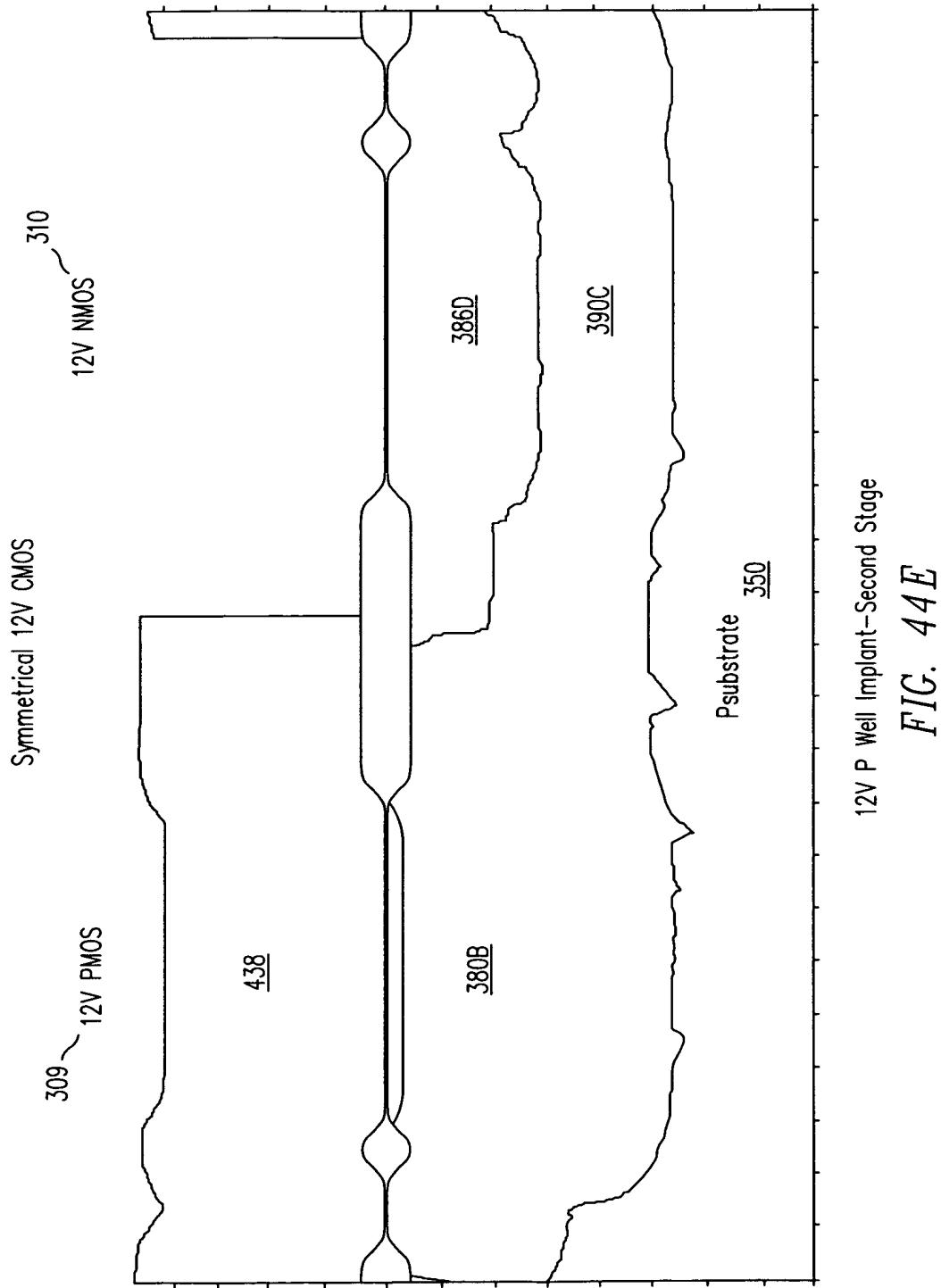


FIG. 44E

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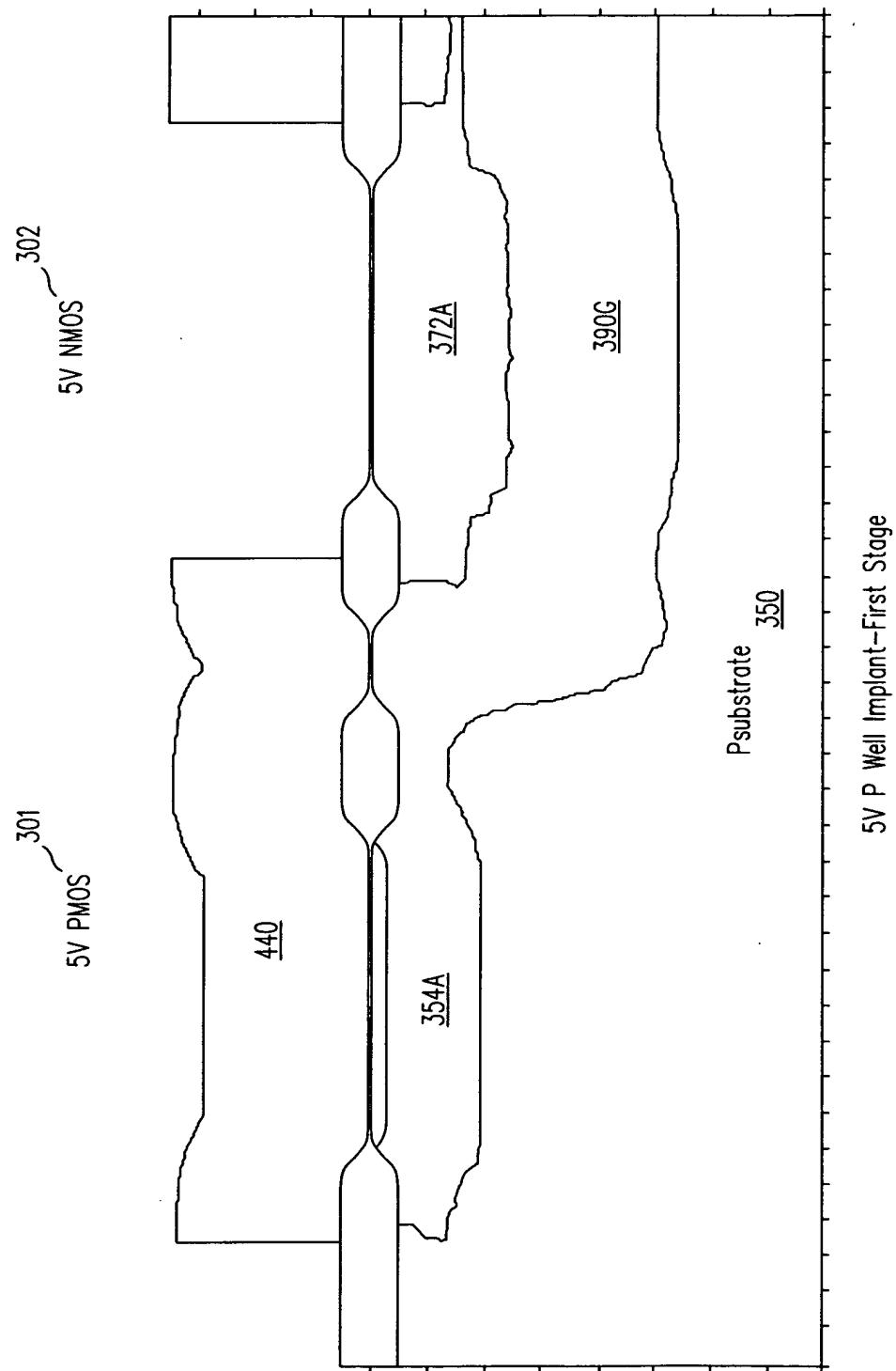
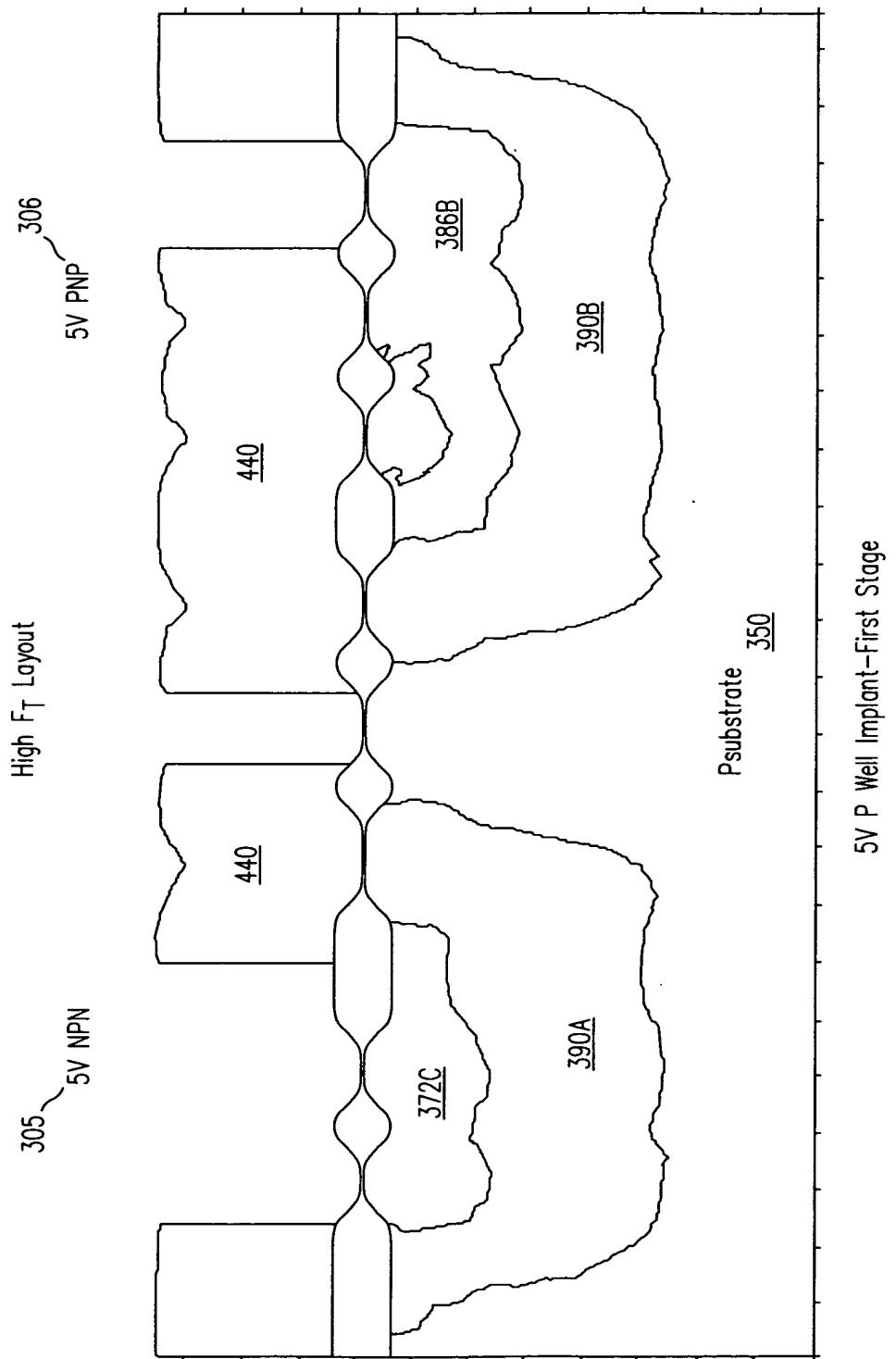
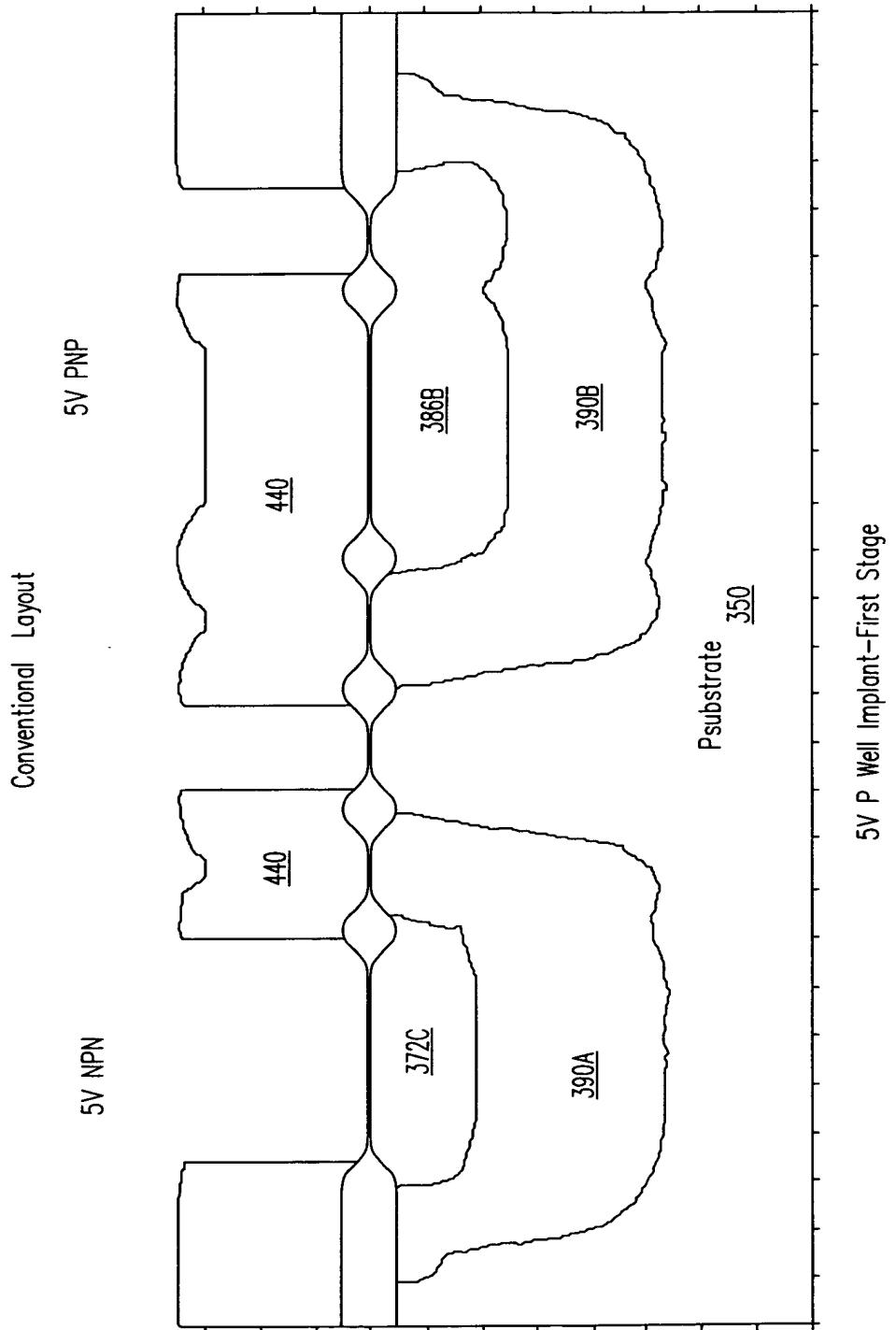


FIG. 45A

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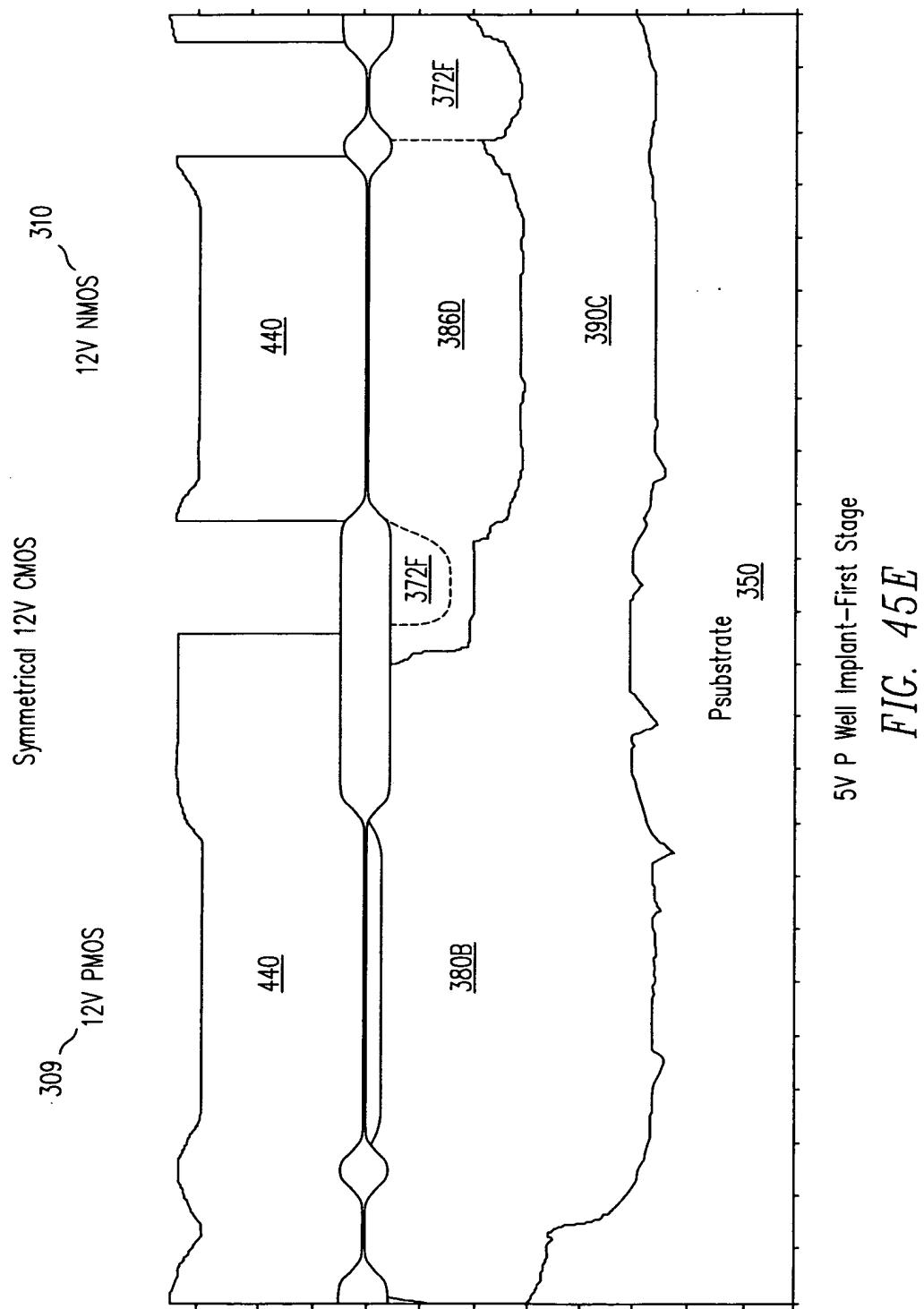




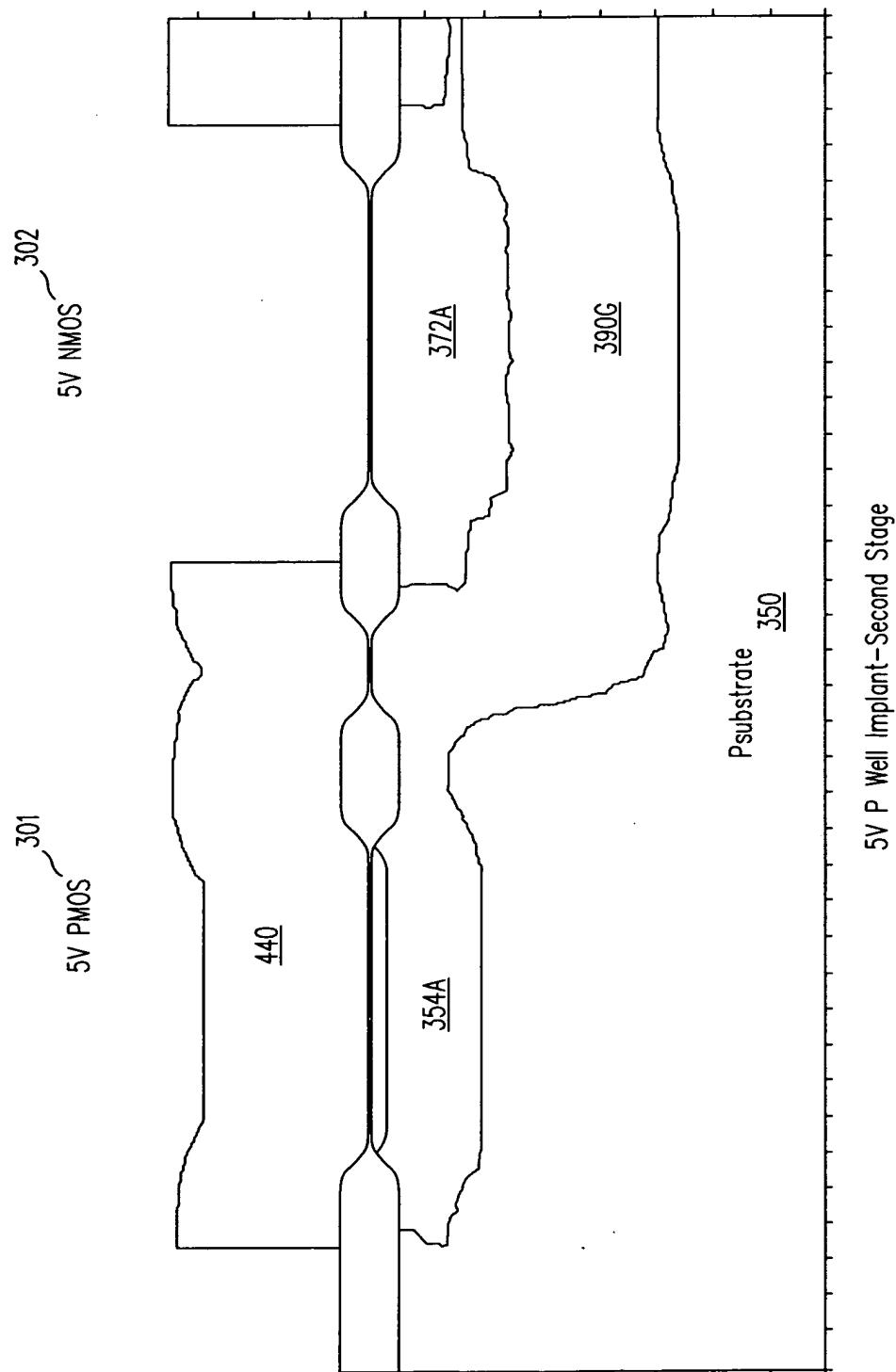
5V P Well Implant-First Stage

FIG. 45C

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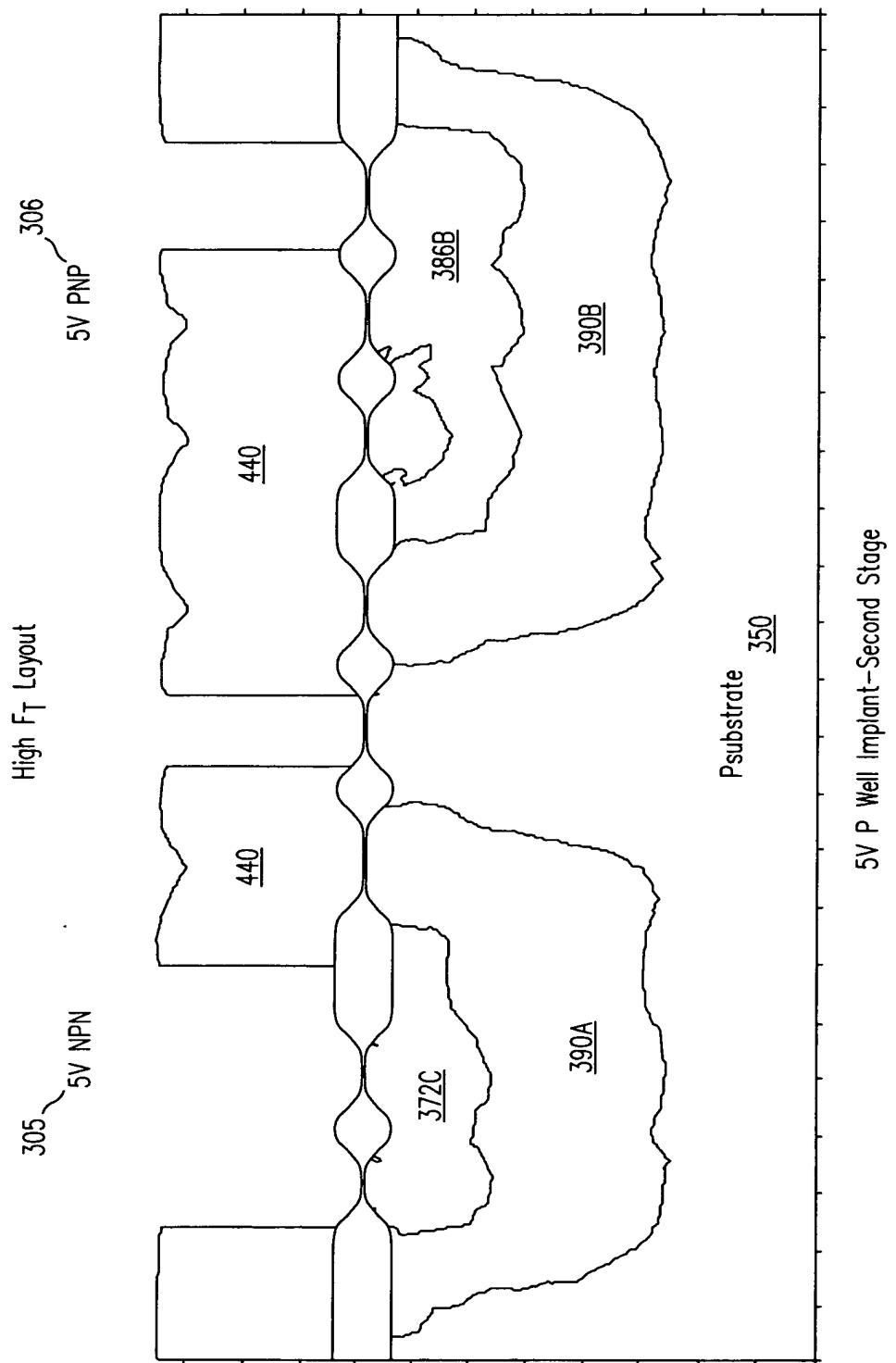


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5V P Well Implant - Second Stage

FIG. 46A



5V P Well Implant—Second Stage

FIG. 46B

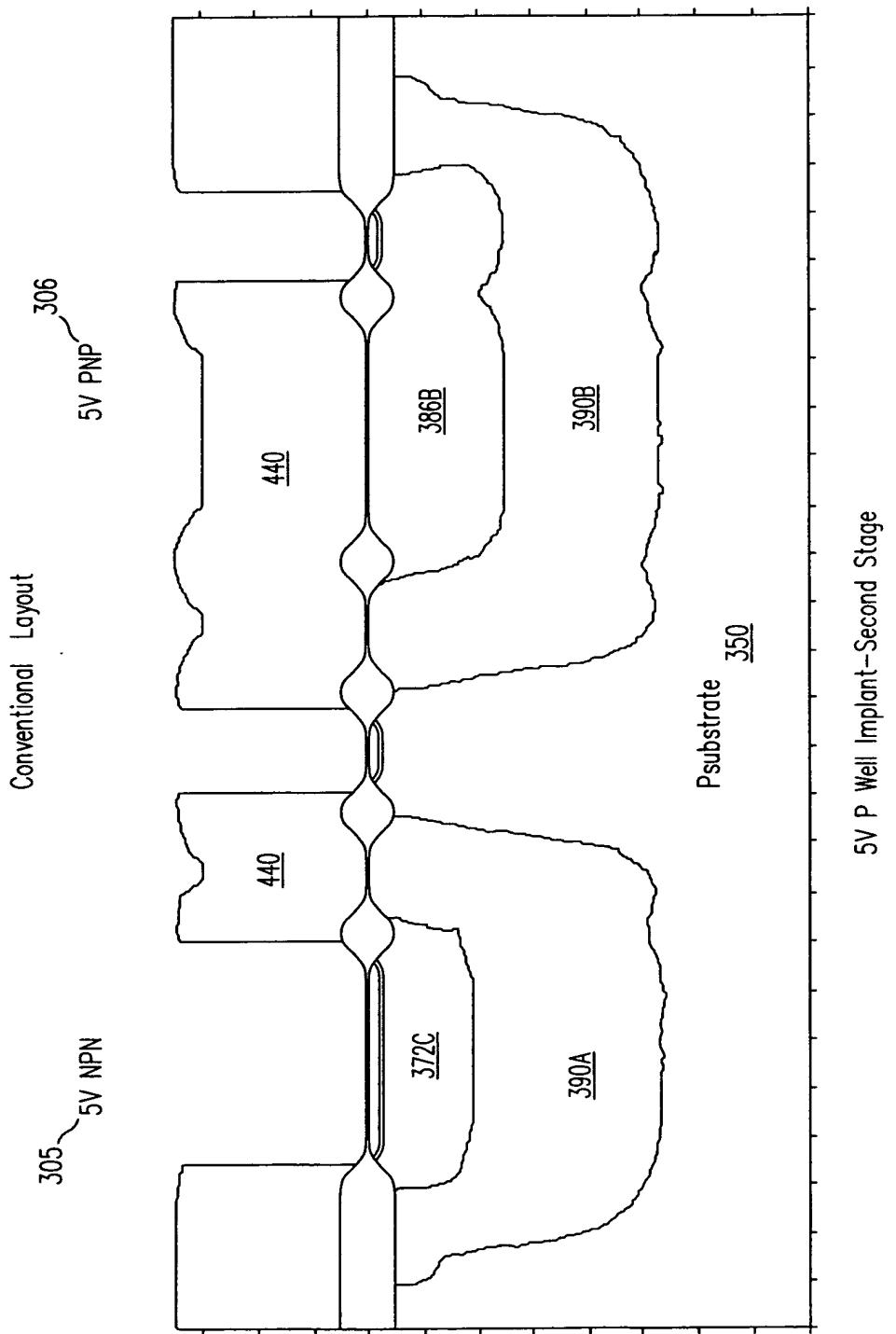
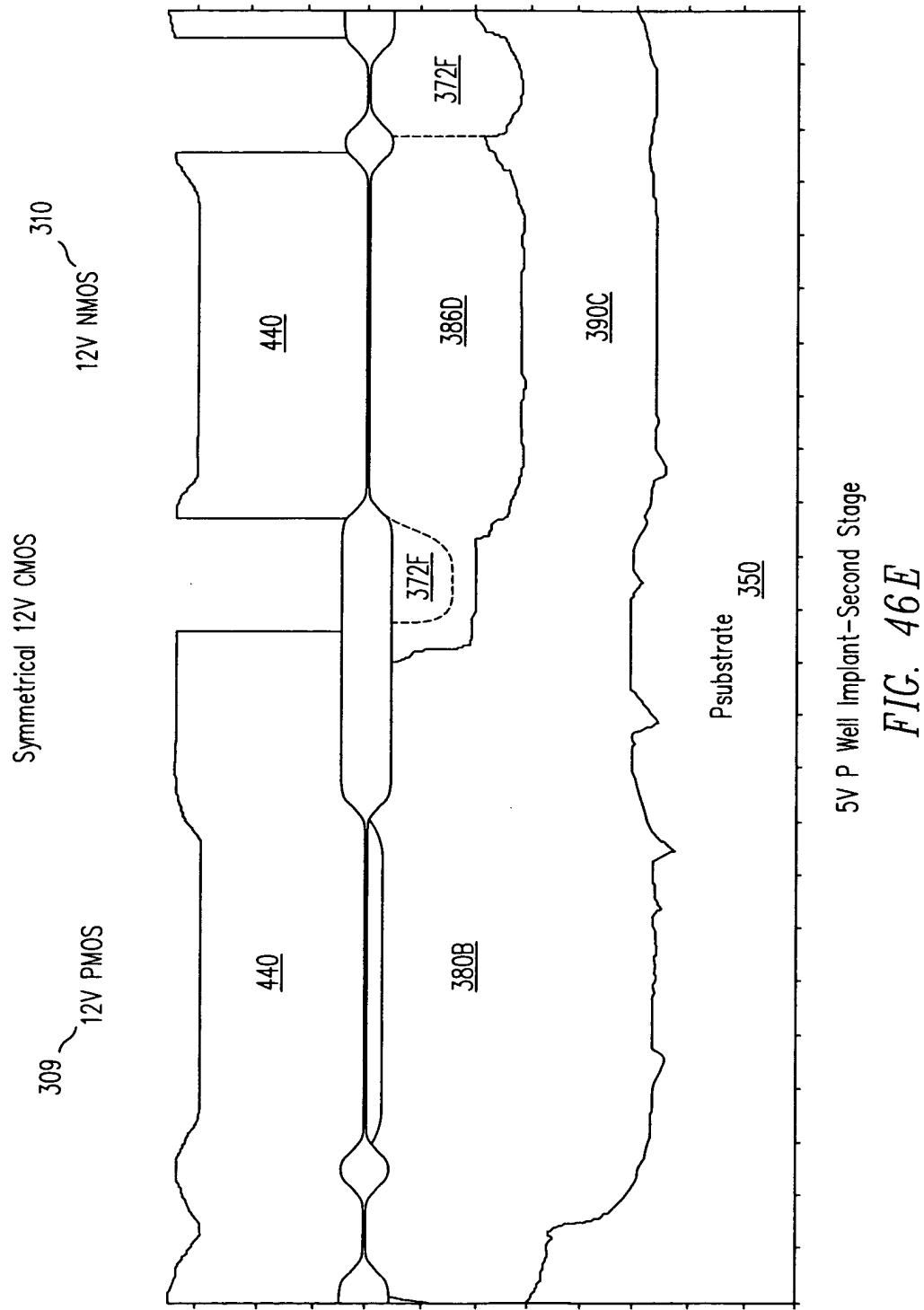


FIG. 46C



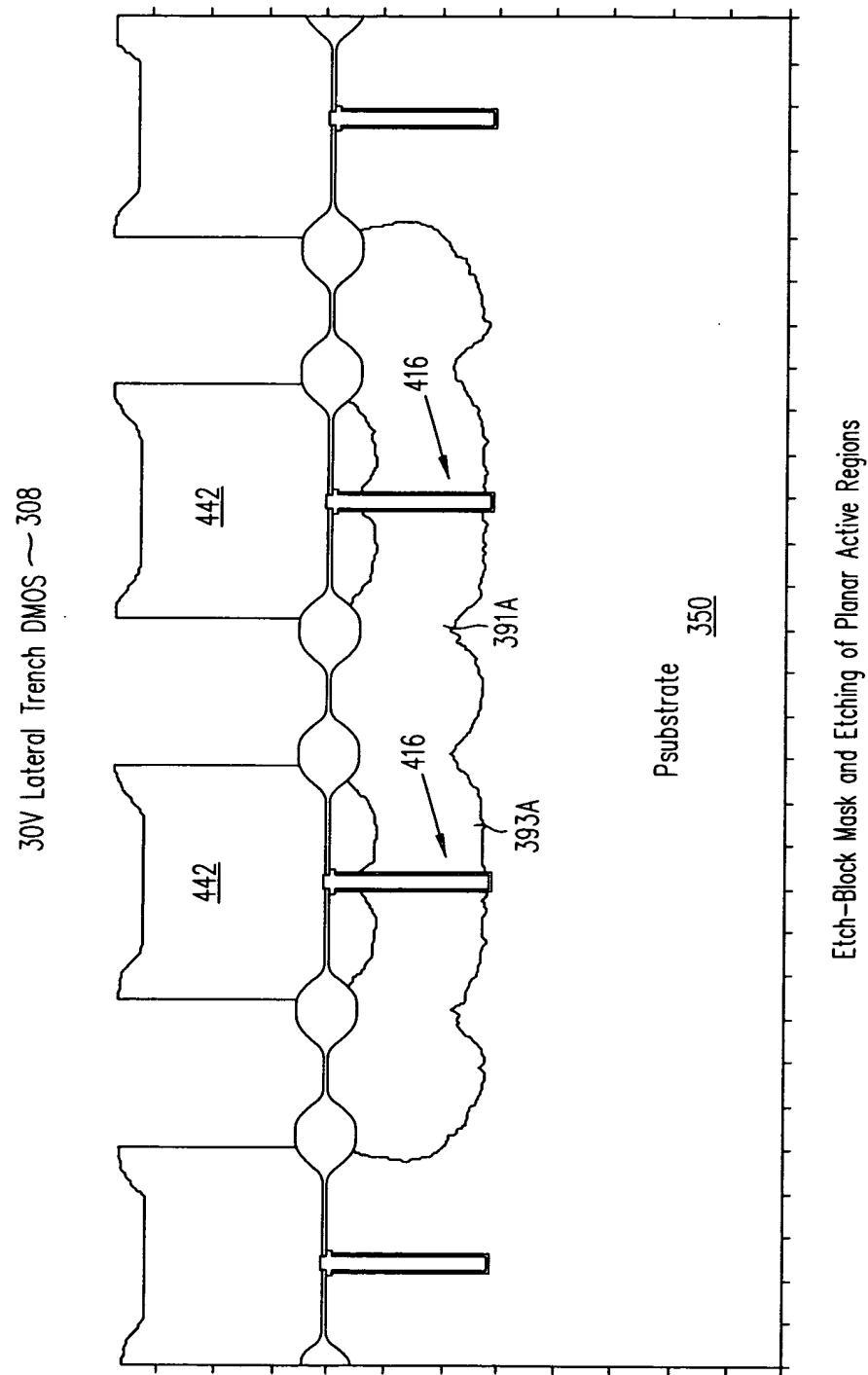


FIG. 47D

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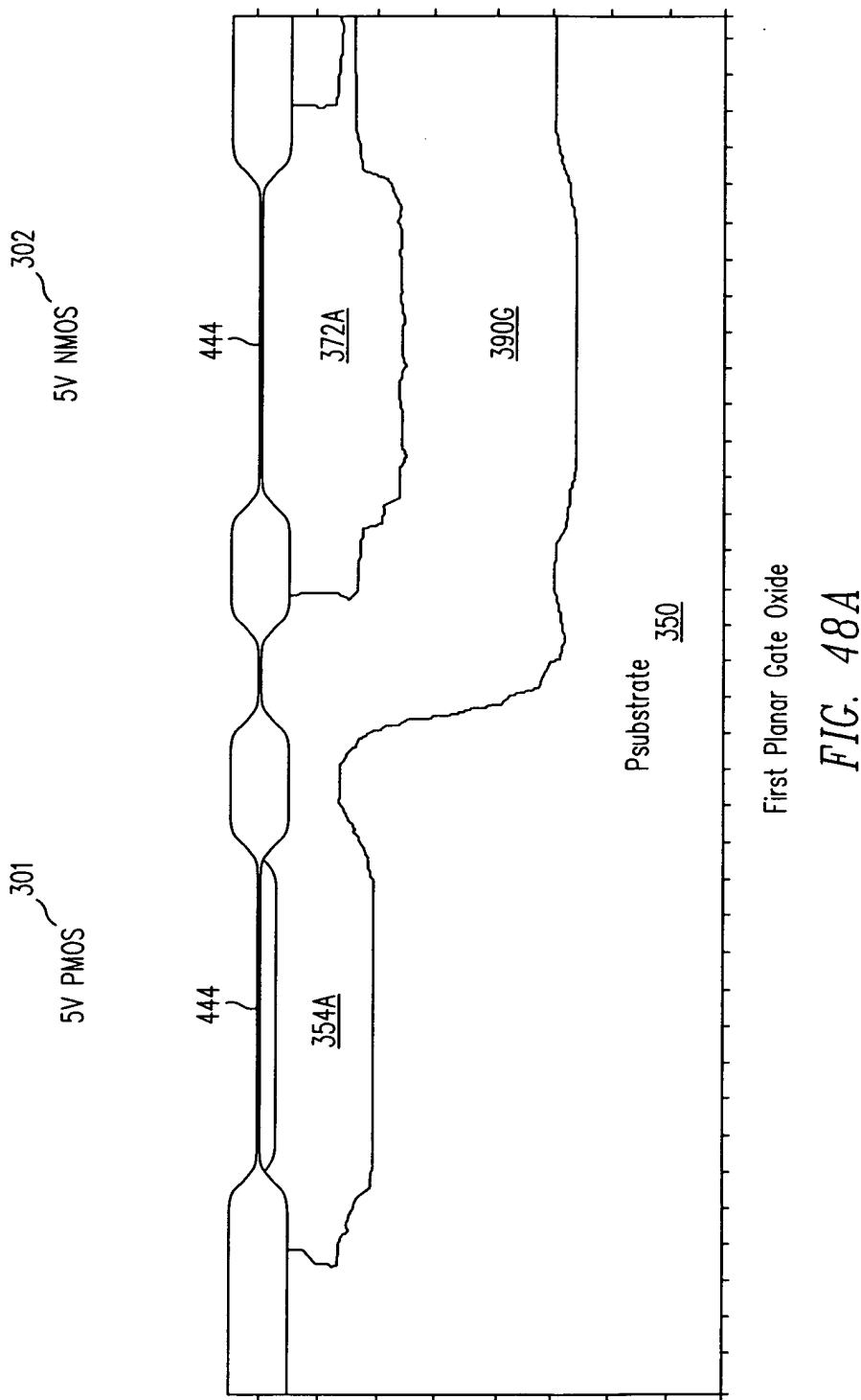


FIG. 48A

First Planar Gate Oxide

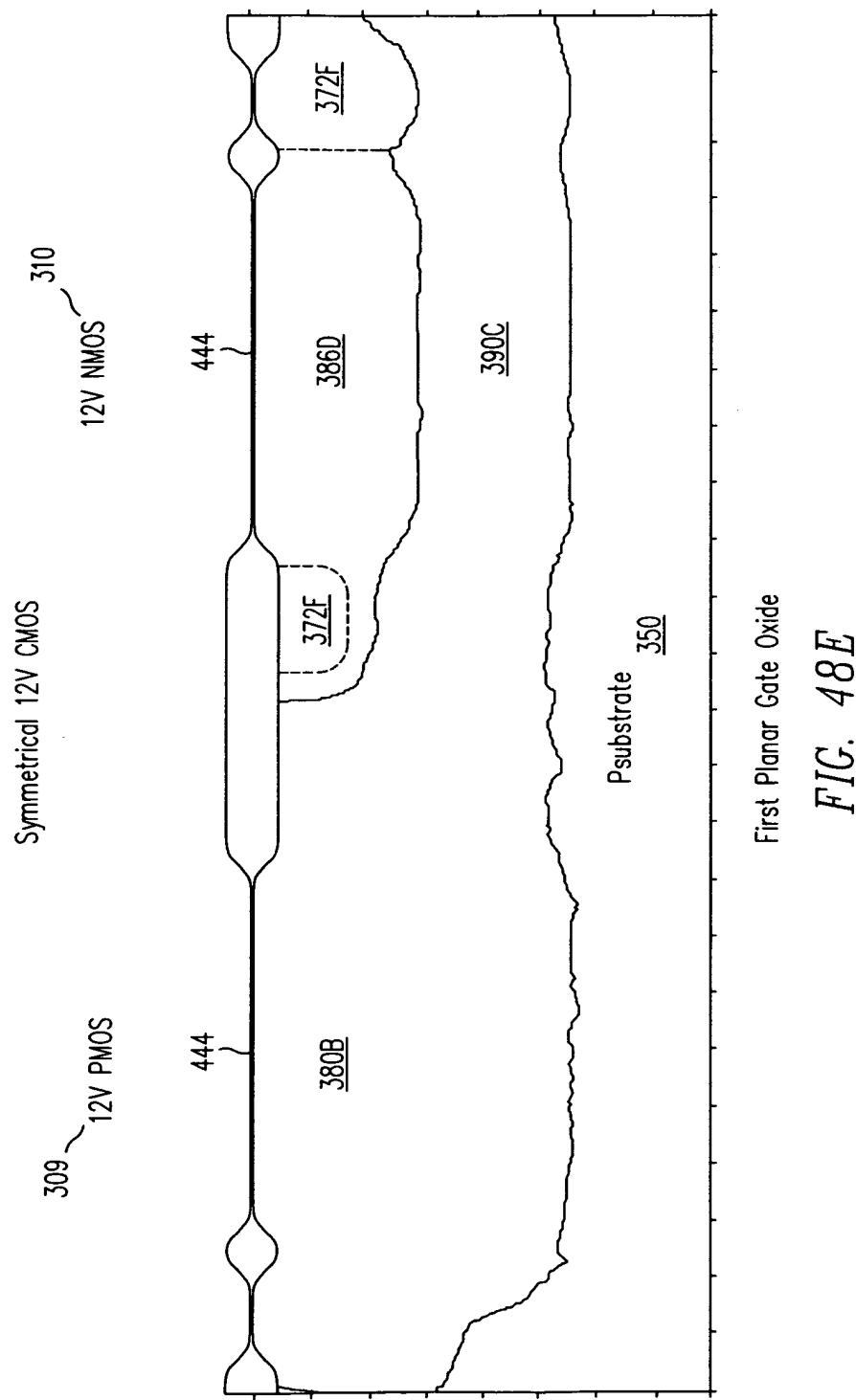
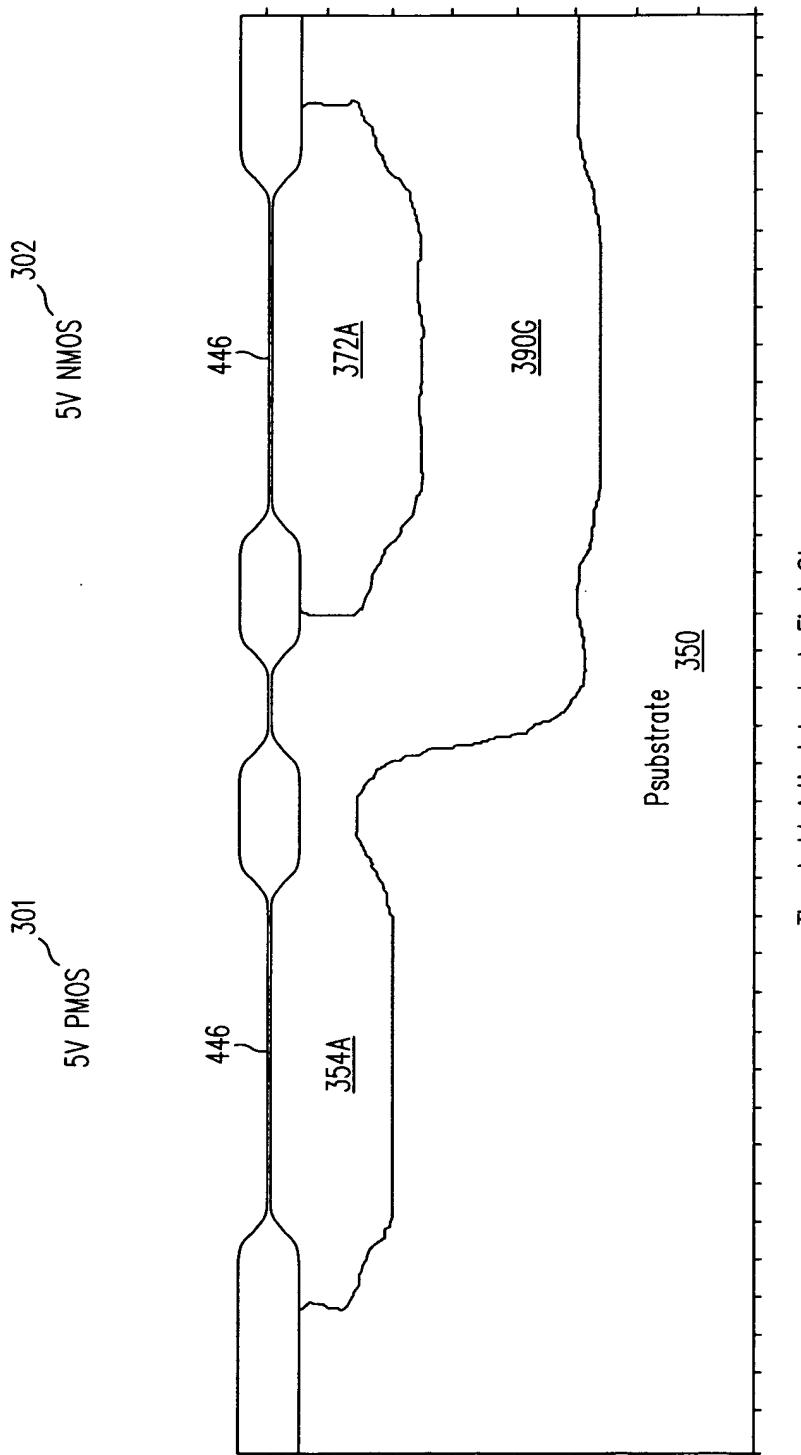


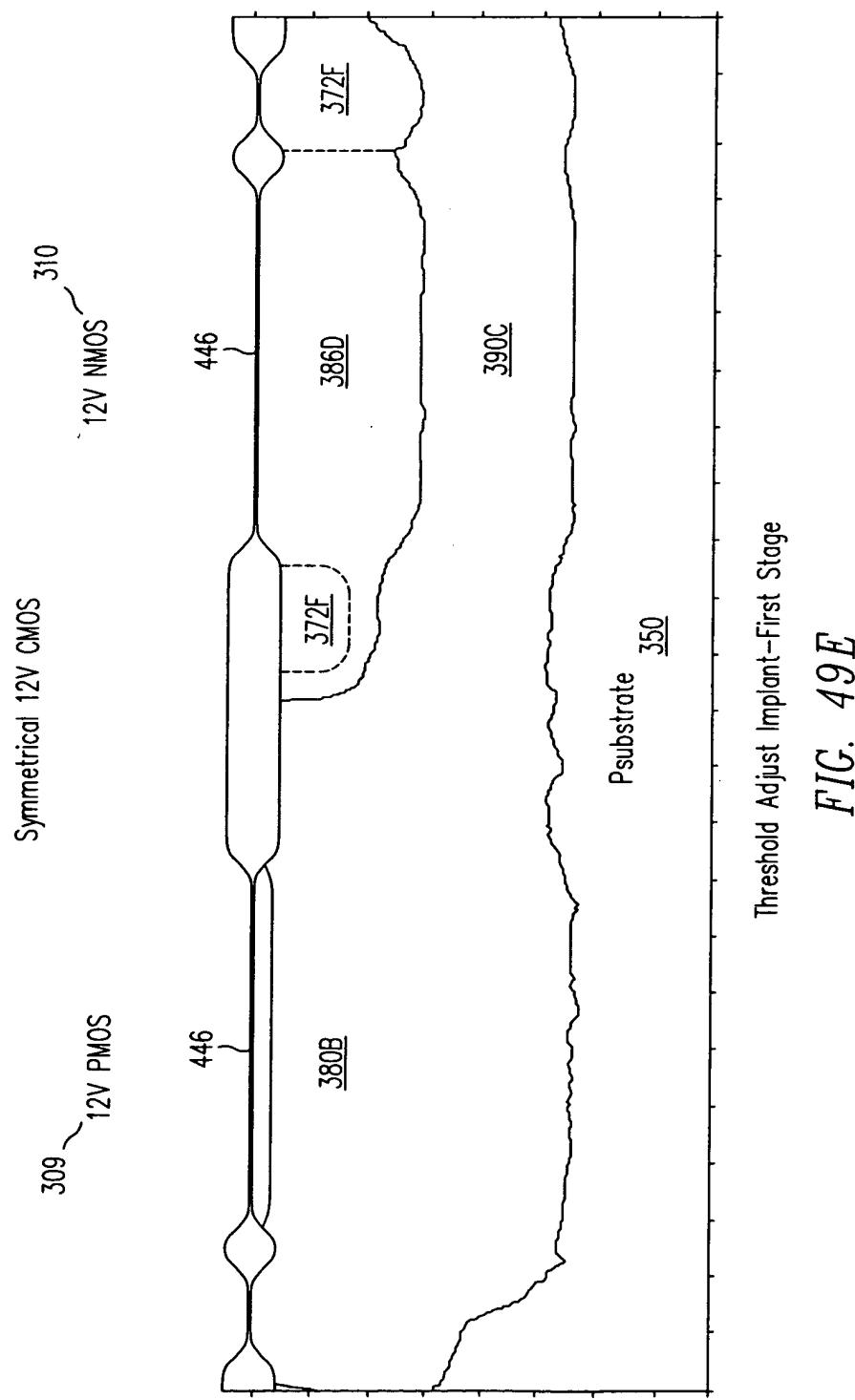
FIG. 48E

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Threshold Adjust Implant-First Stage

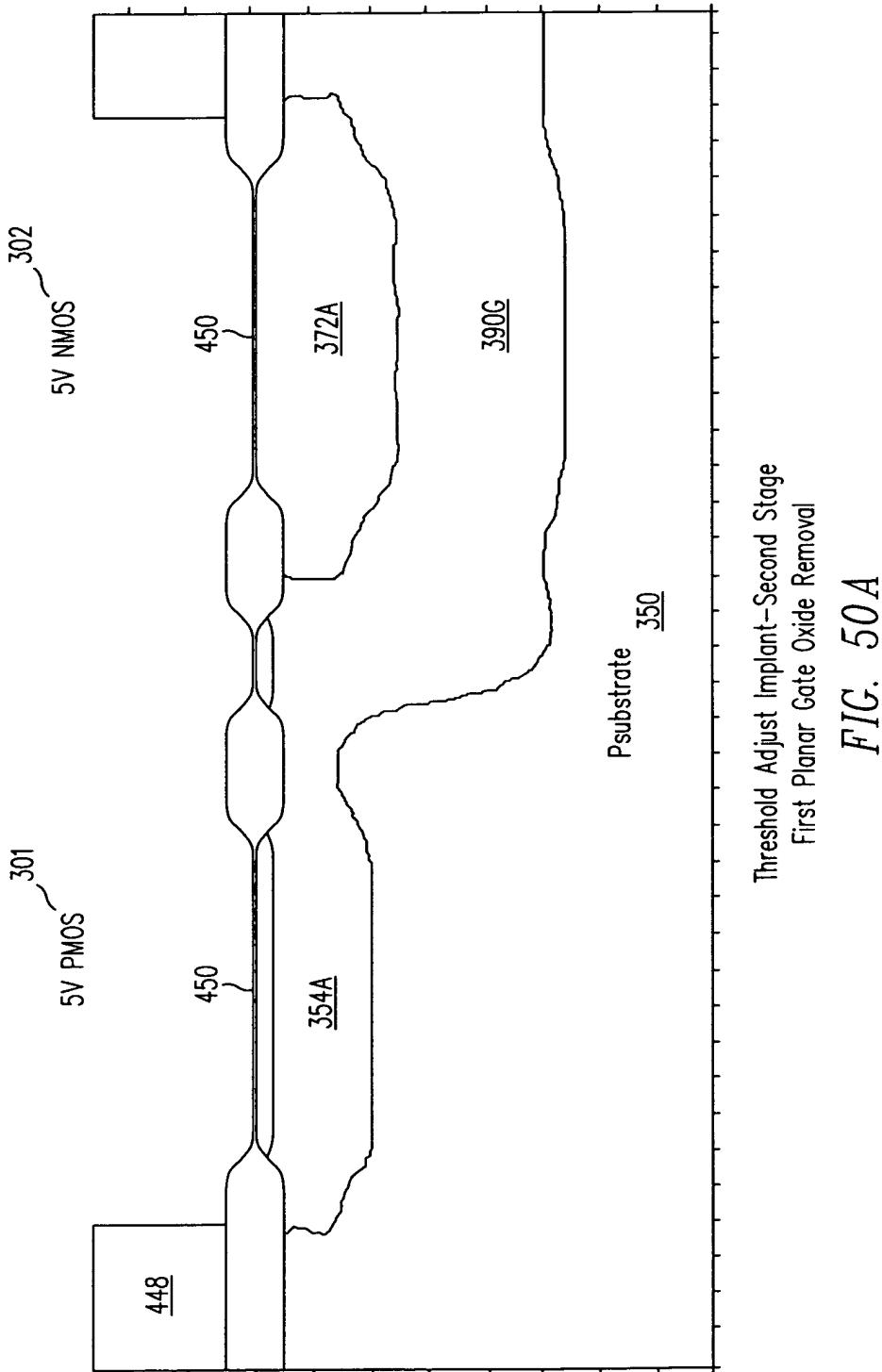
FIG. 49A



Threshold Adjust Implant-First Stage

FIG. 49E

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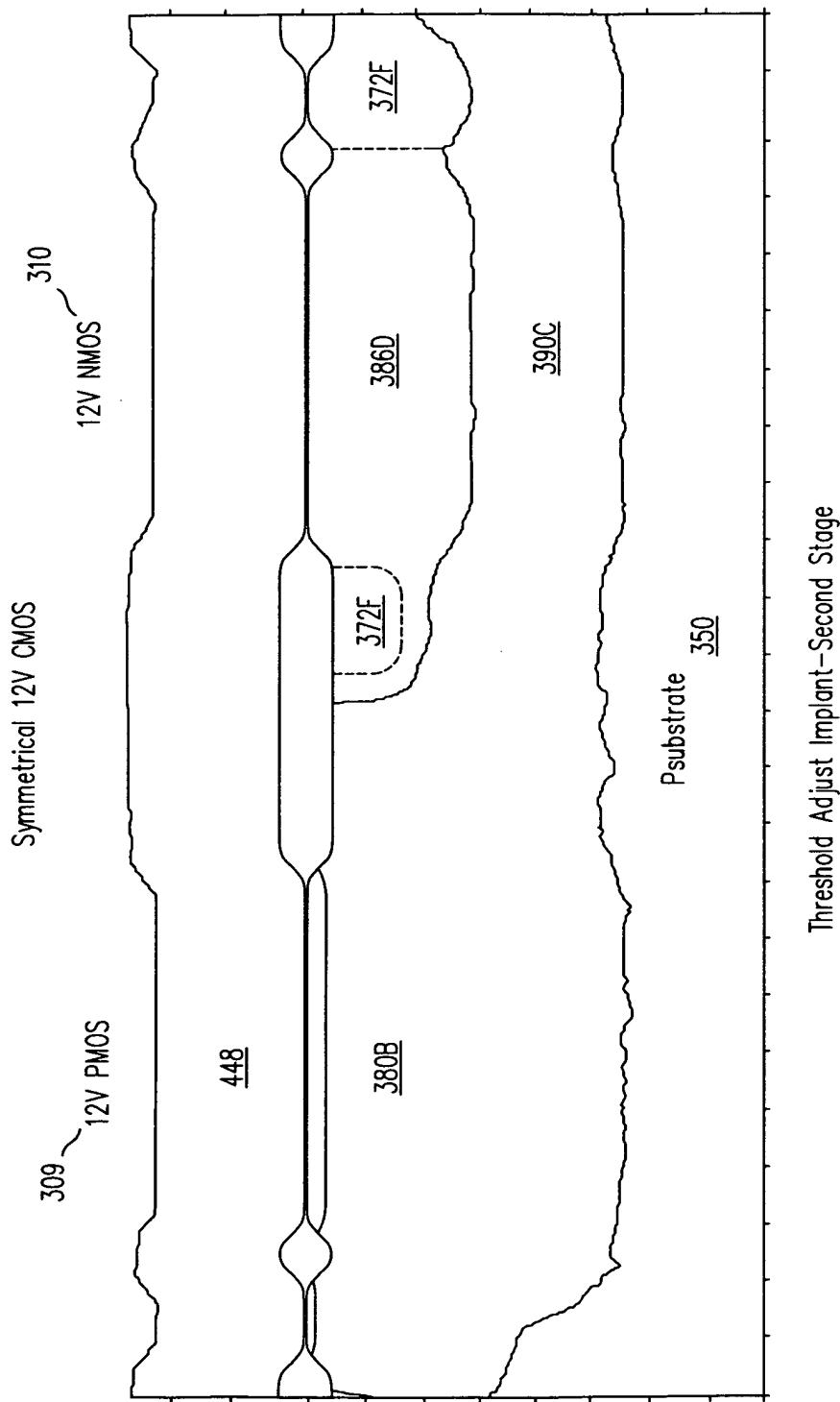
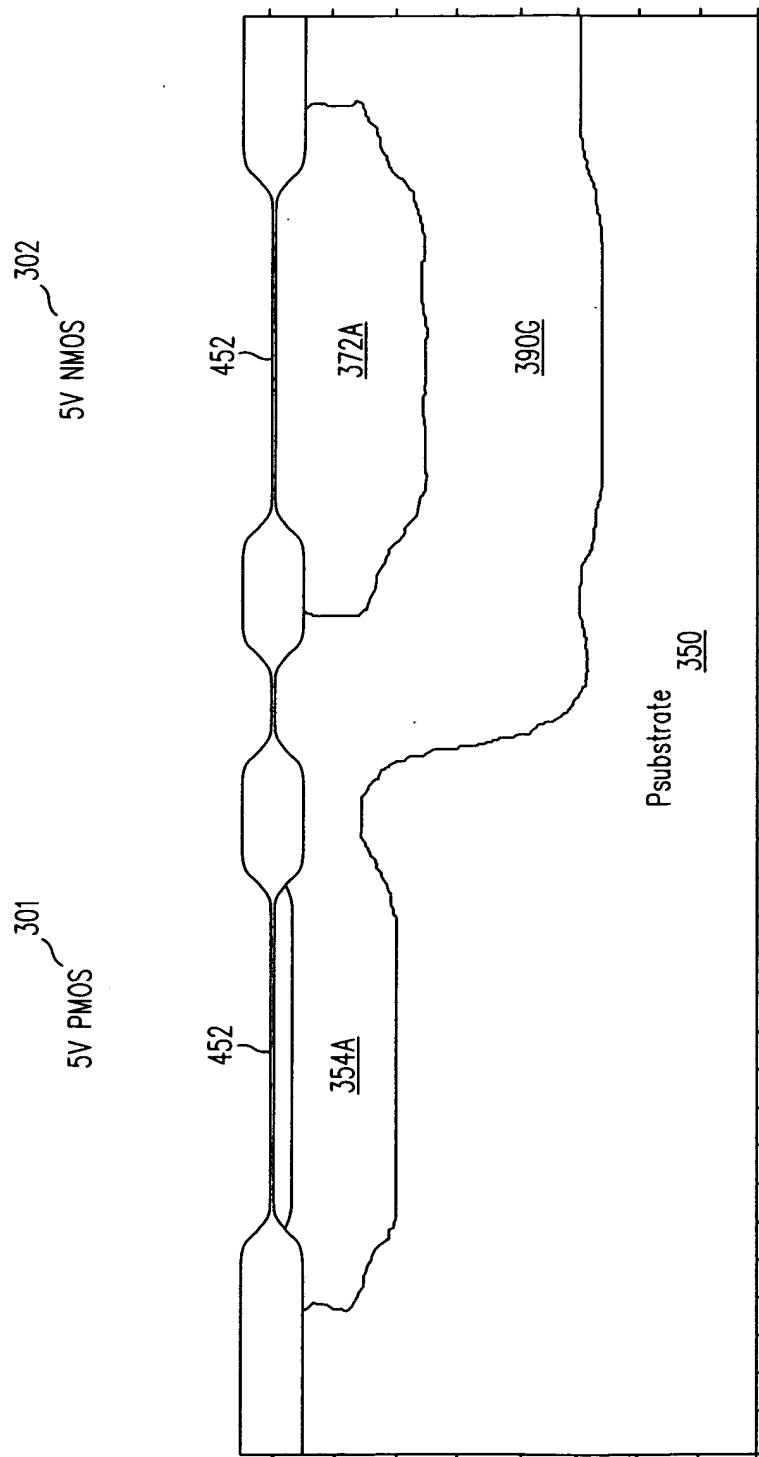


FIG. 50E

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Second Planar Gate Oxide

FIG. 51A

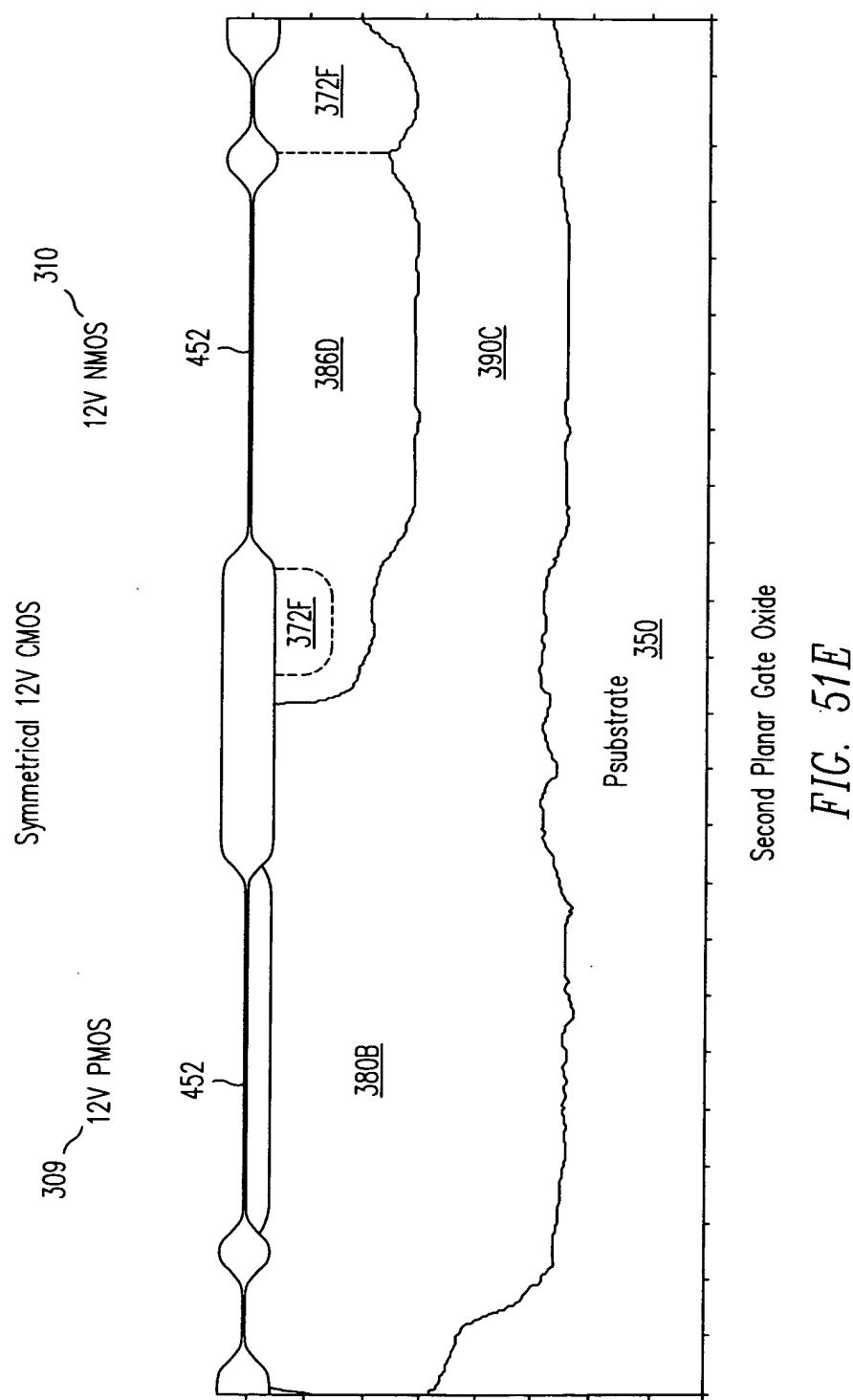


FIG. 51E

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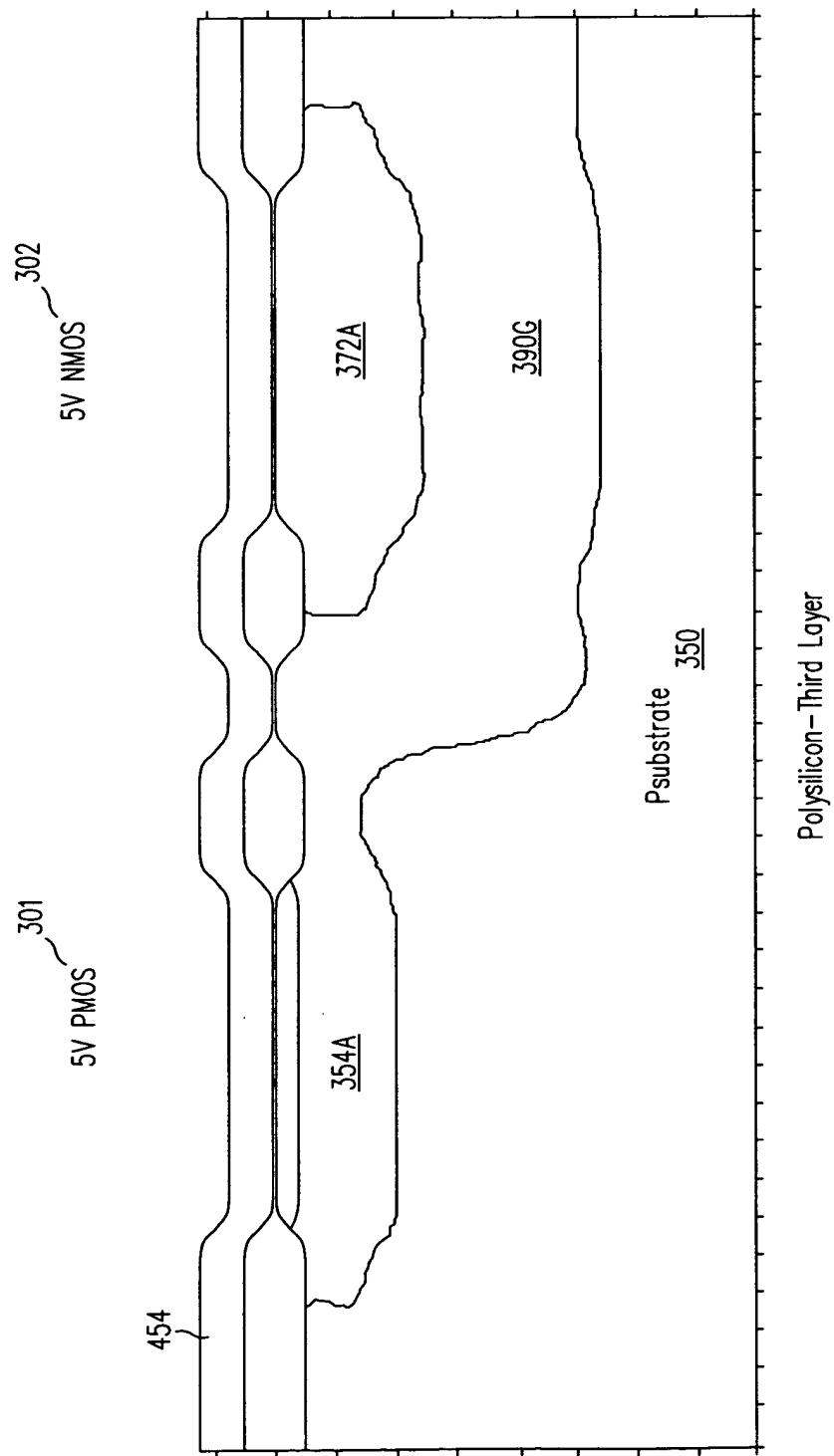
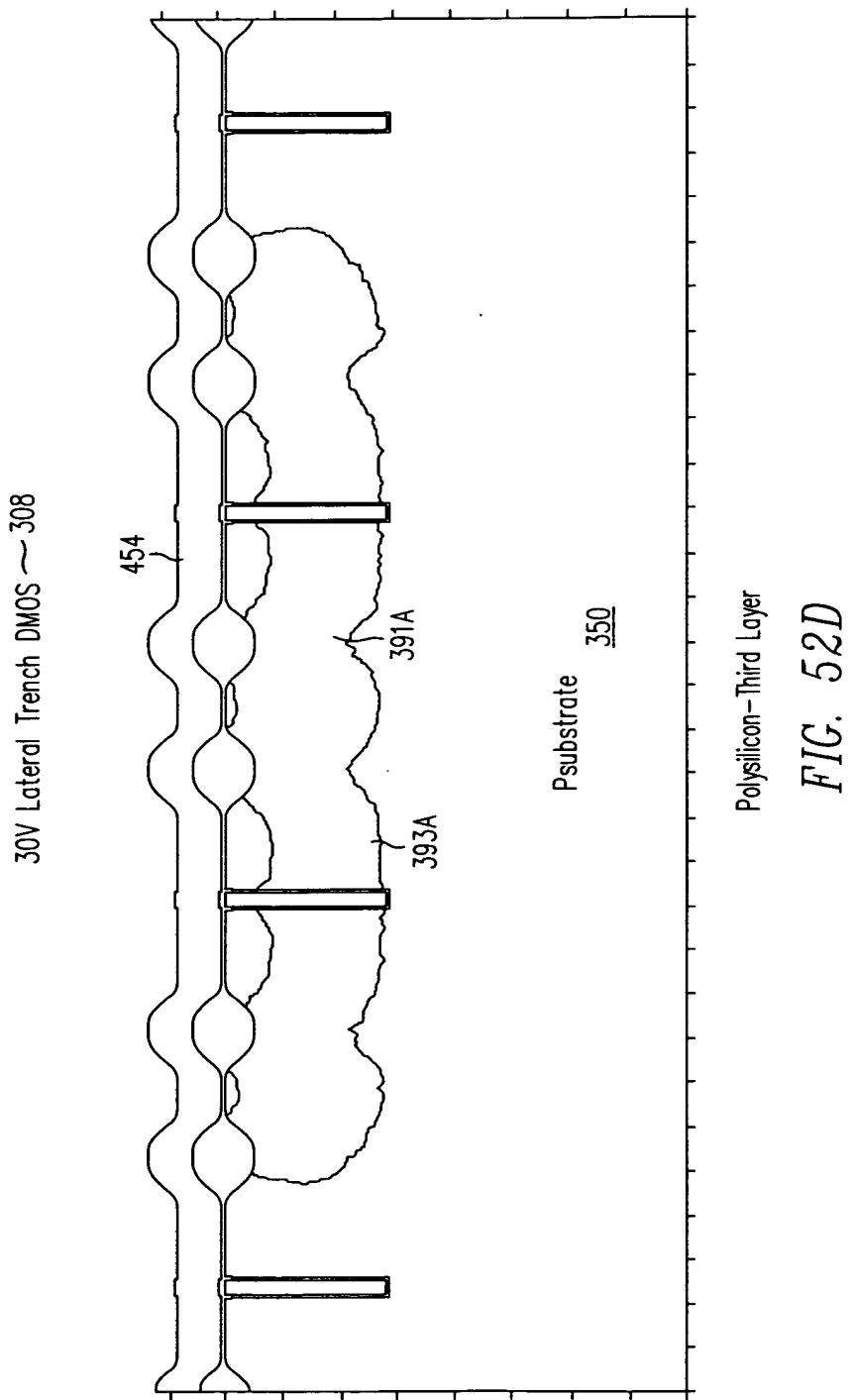


FIG. 52A

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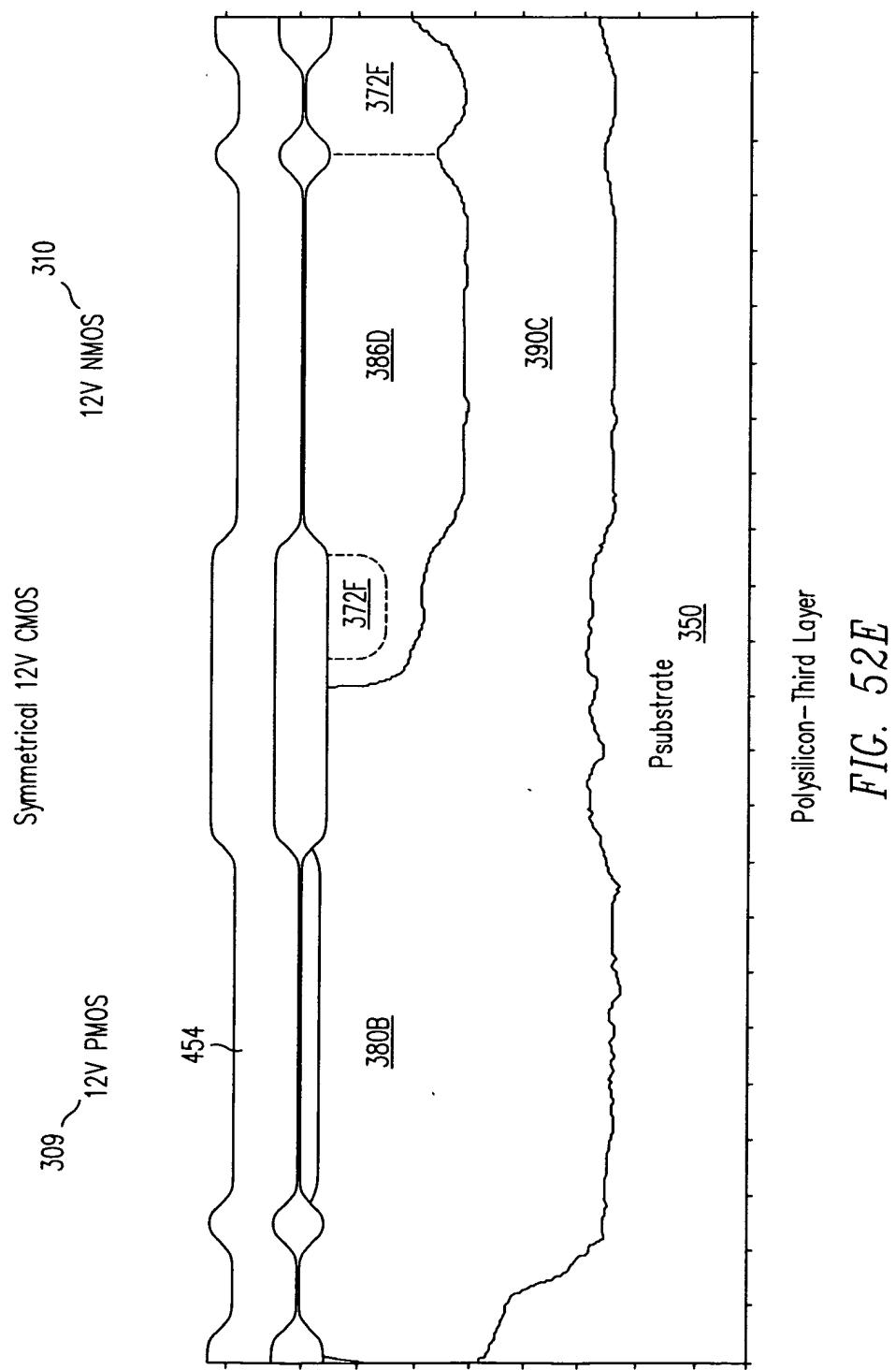
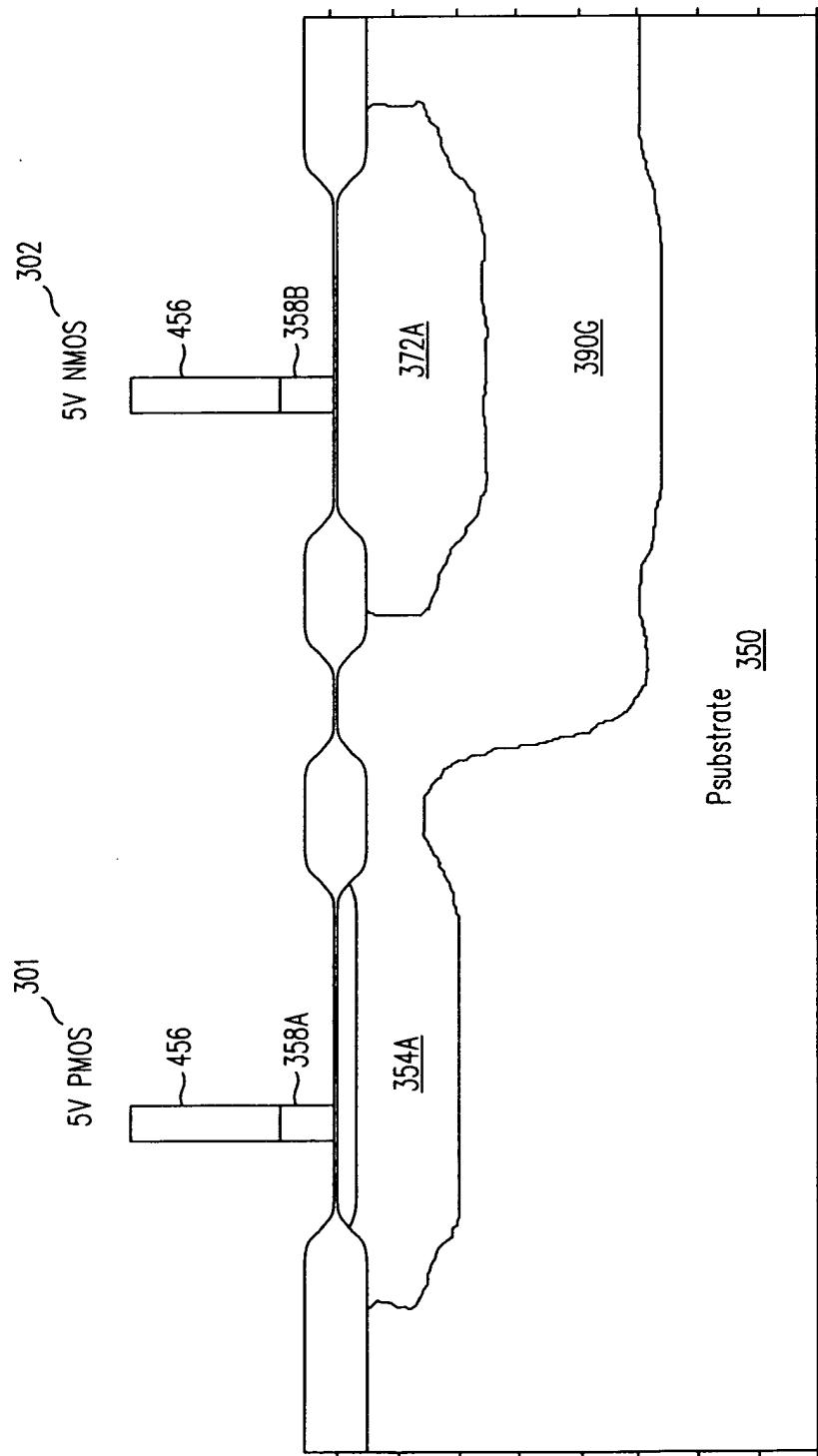


FIG. 52E

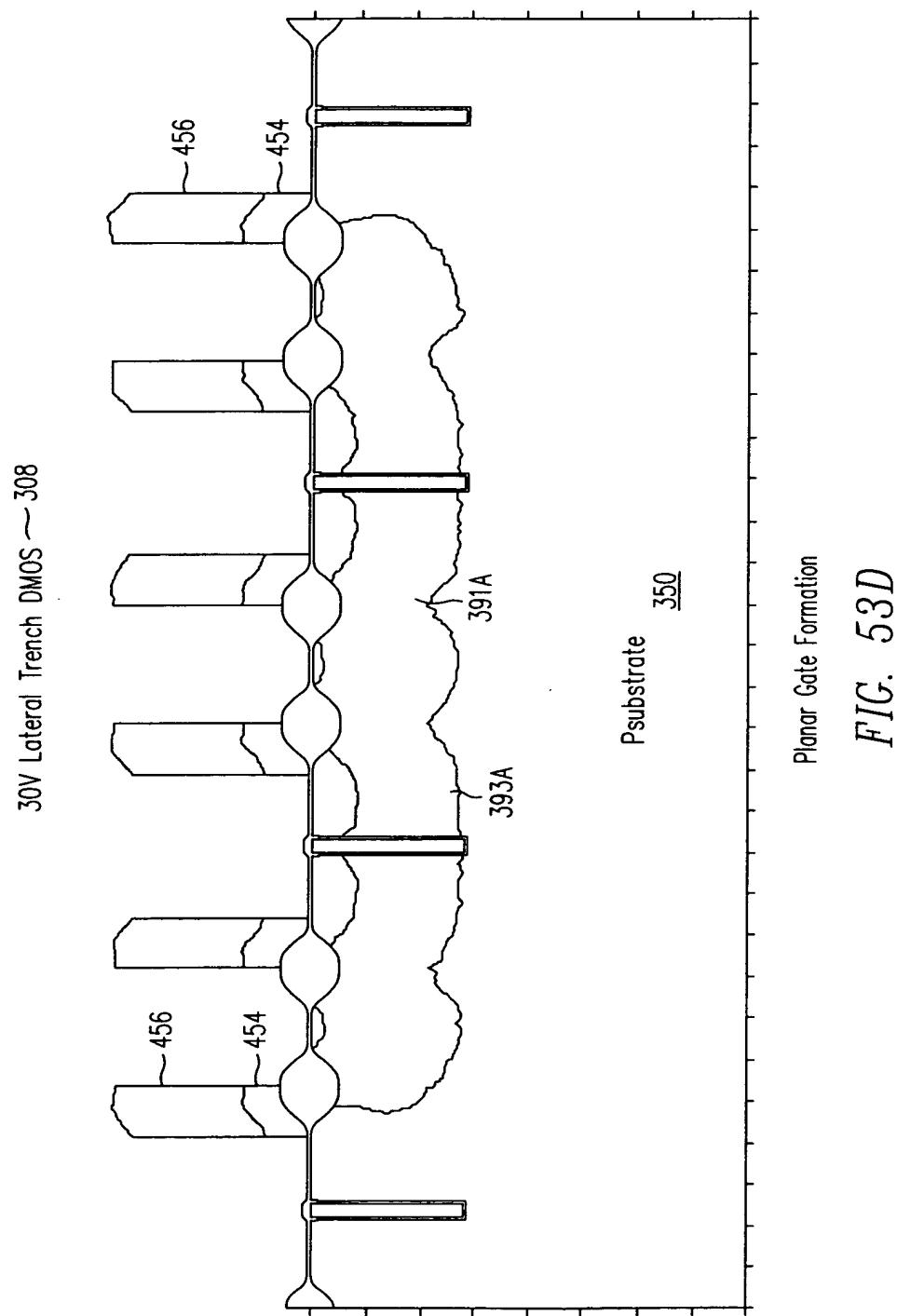
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Planar Gate Formation

FIG. 53A

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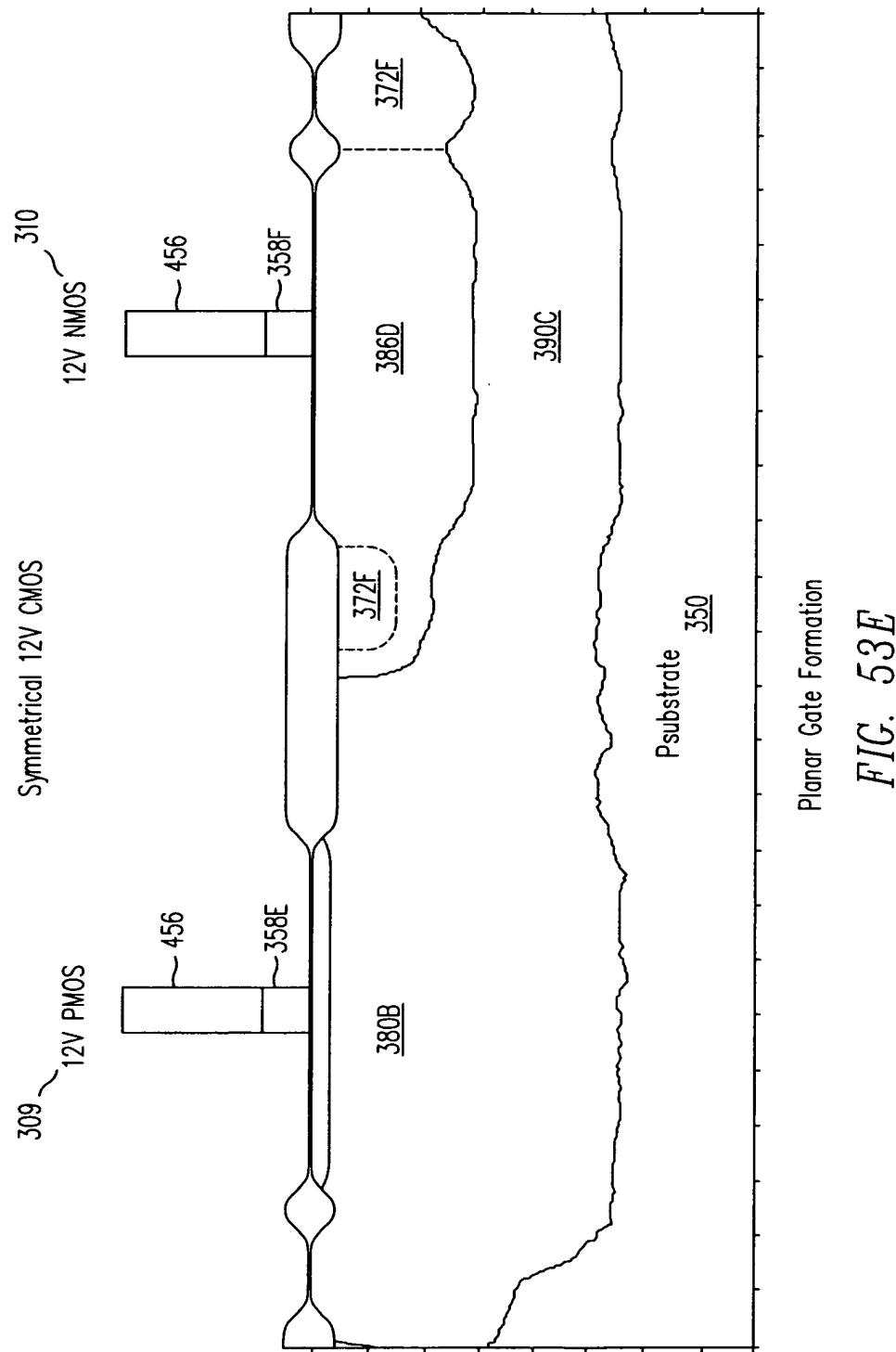
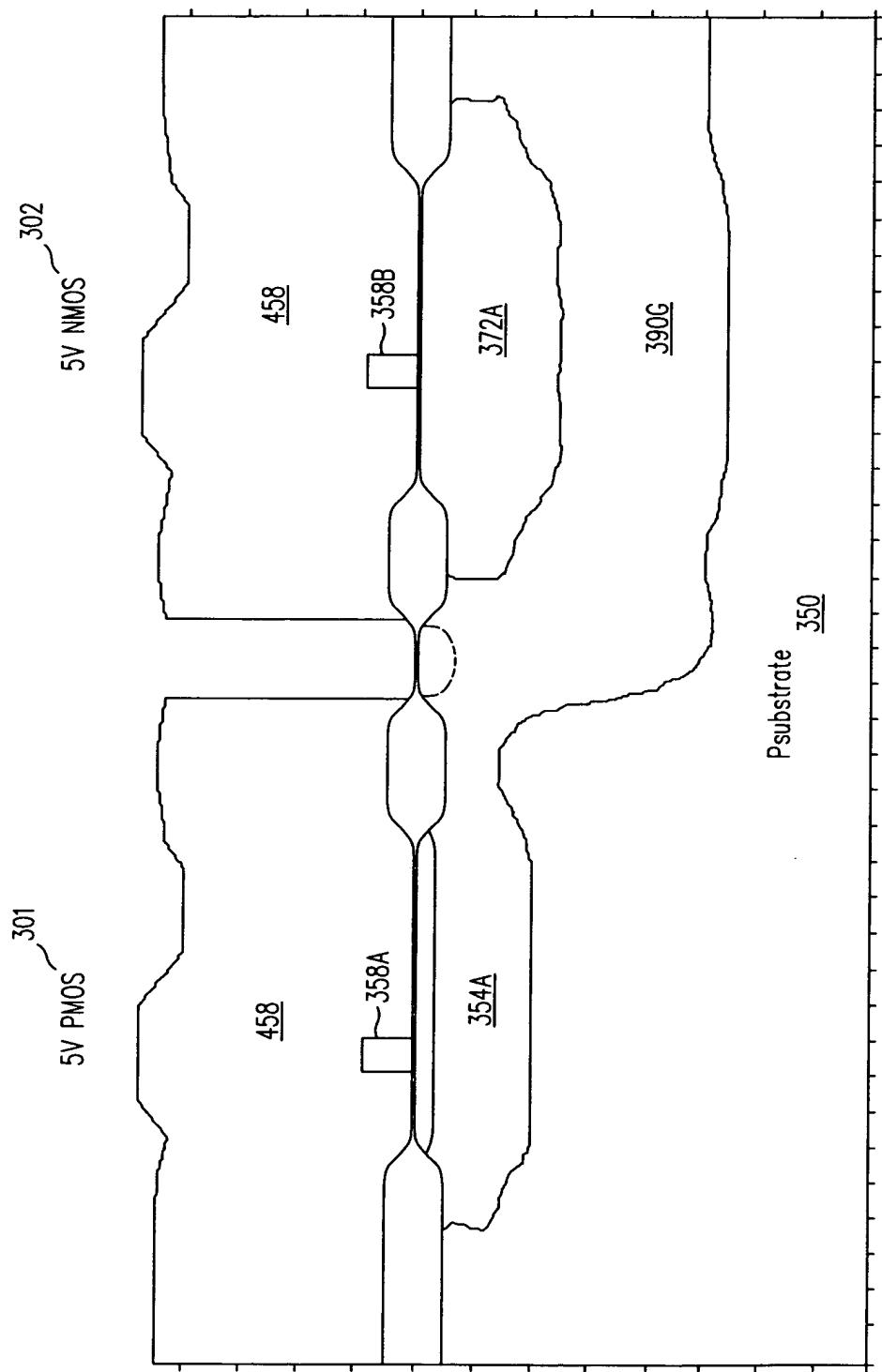


FIG. 53E

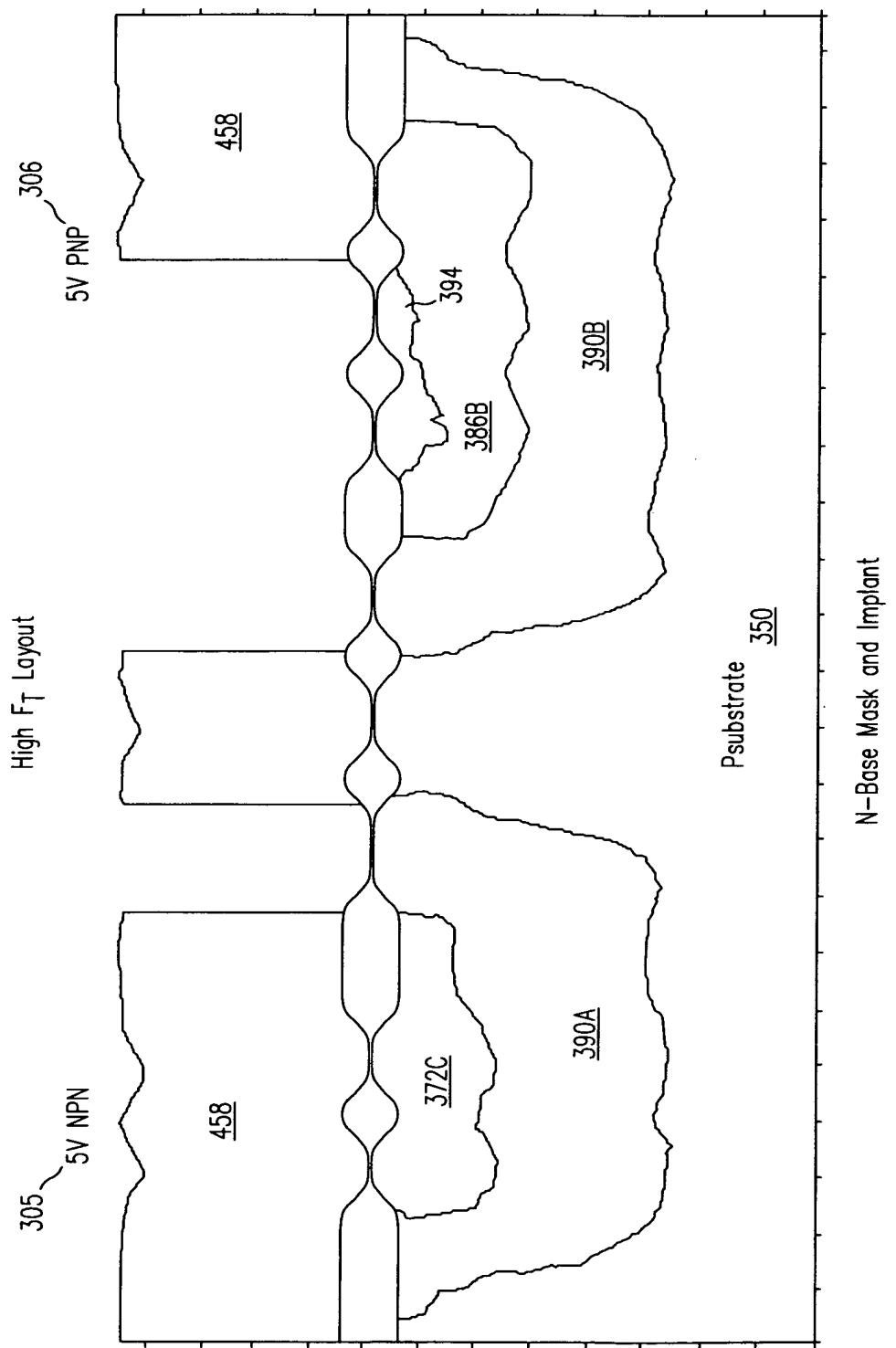
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N-Base Mask and Implant

FIG. 54A

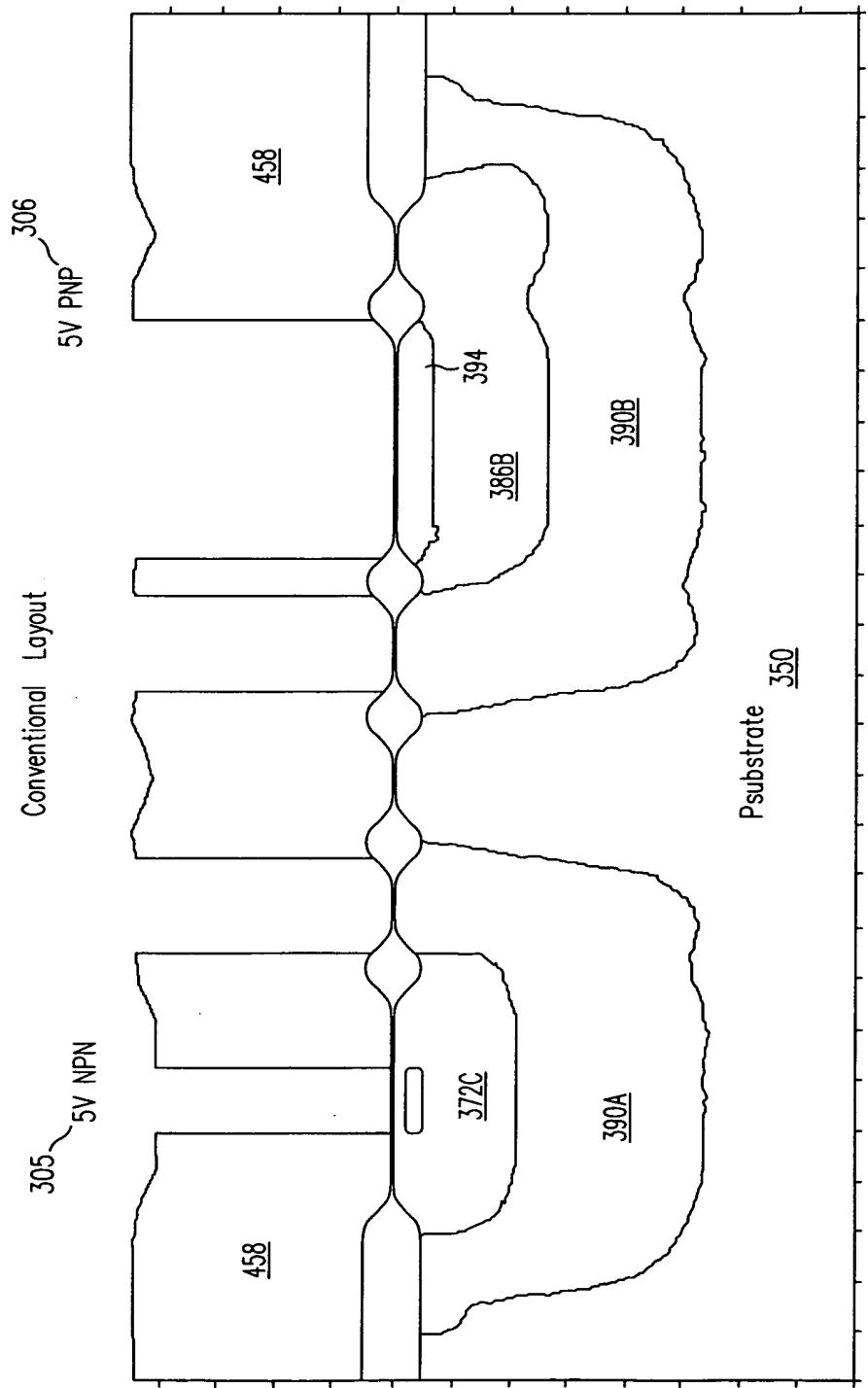
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N-Base Mask and Implant

FIG. 54B

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N-Base Mask and Implant
FIG. 54C

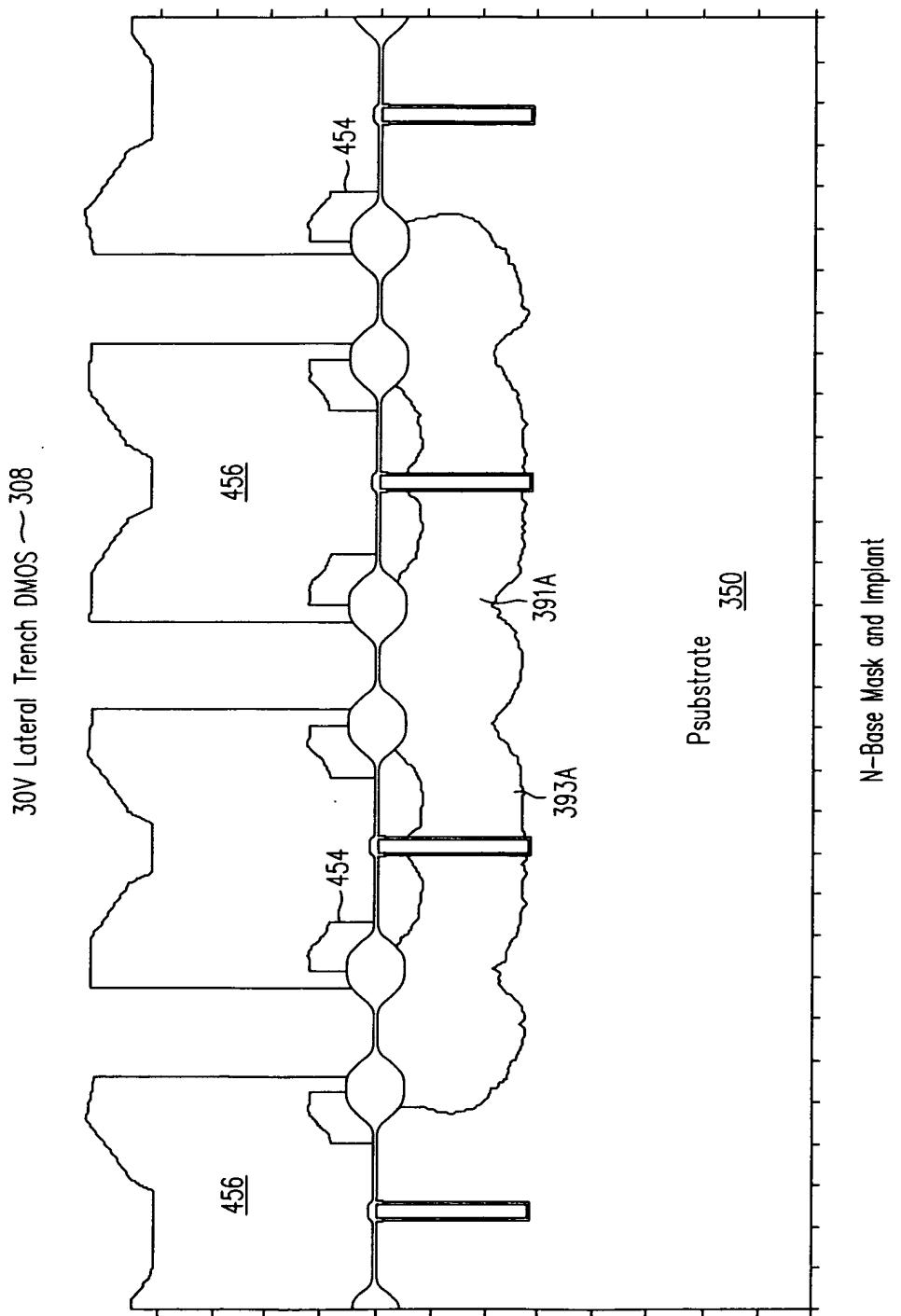
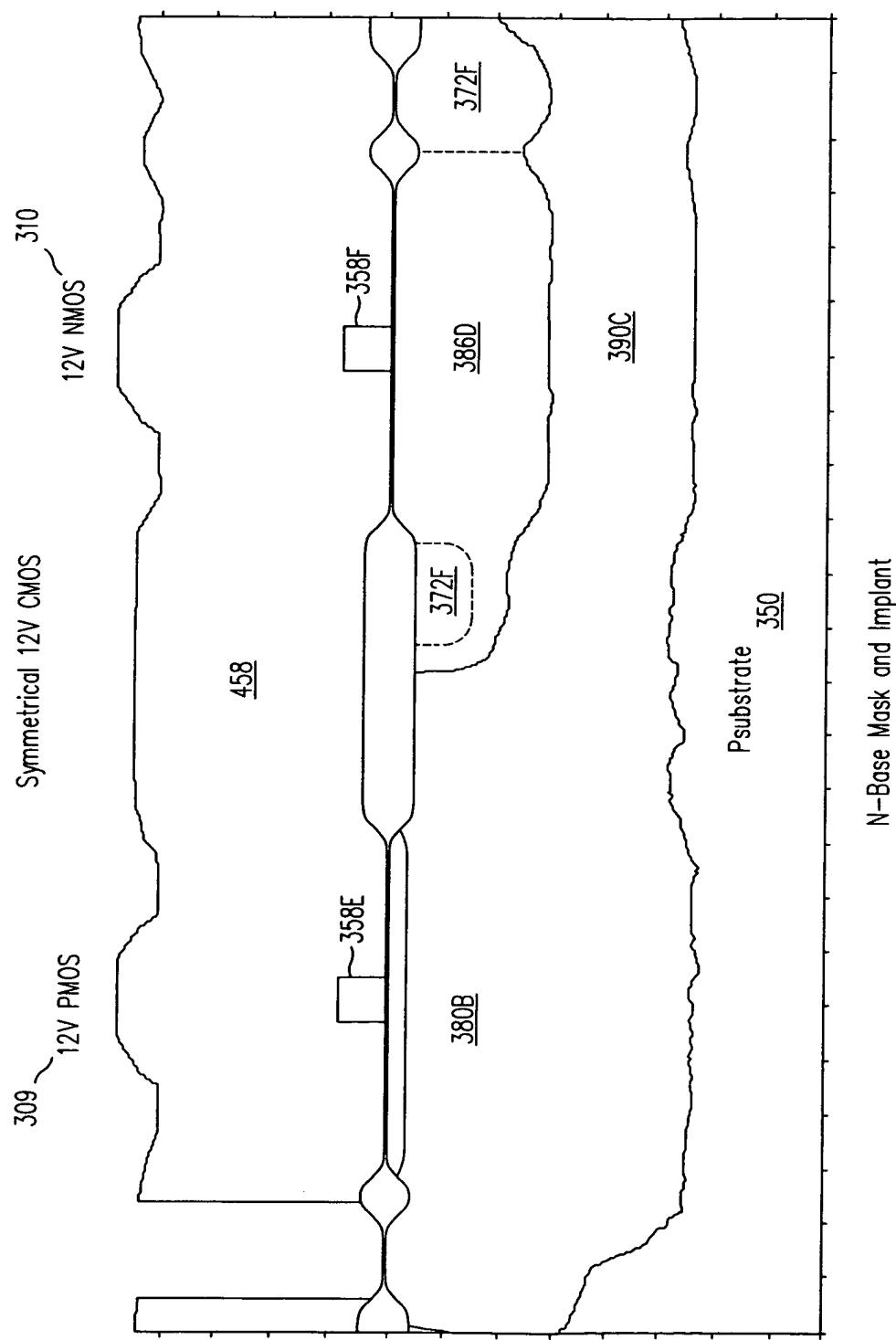


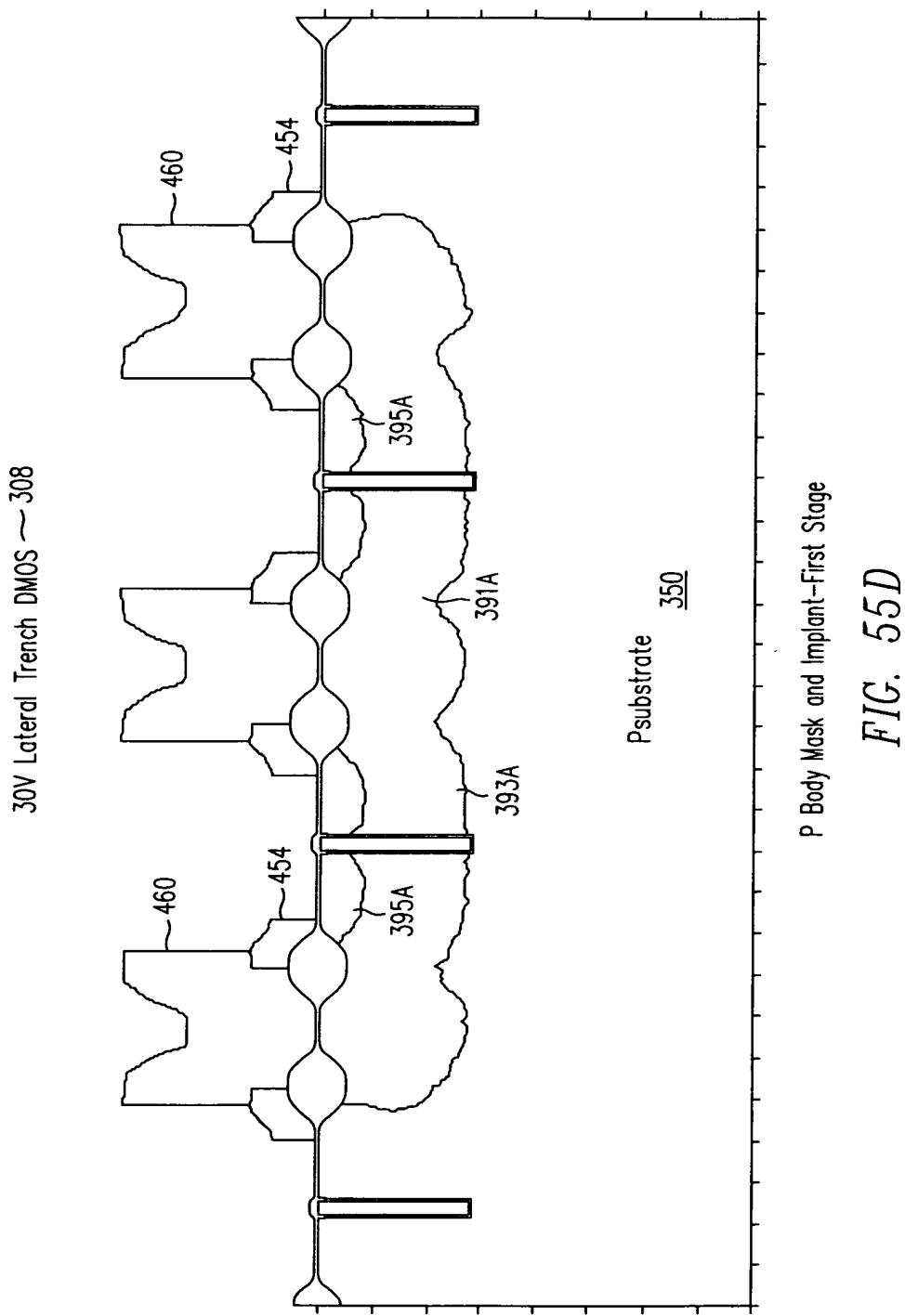
FIG. 54D

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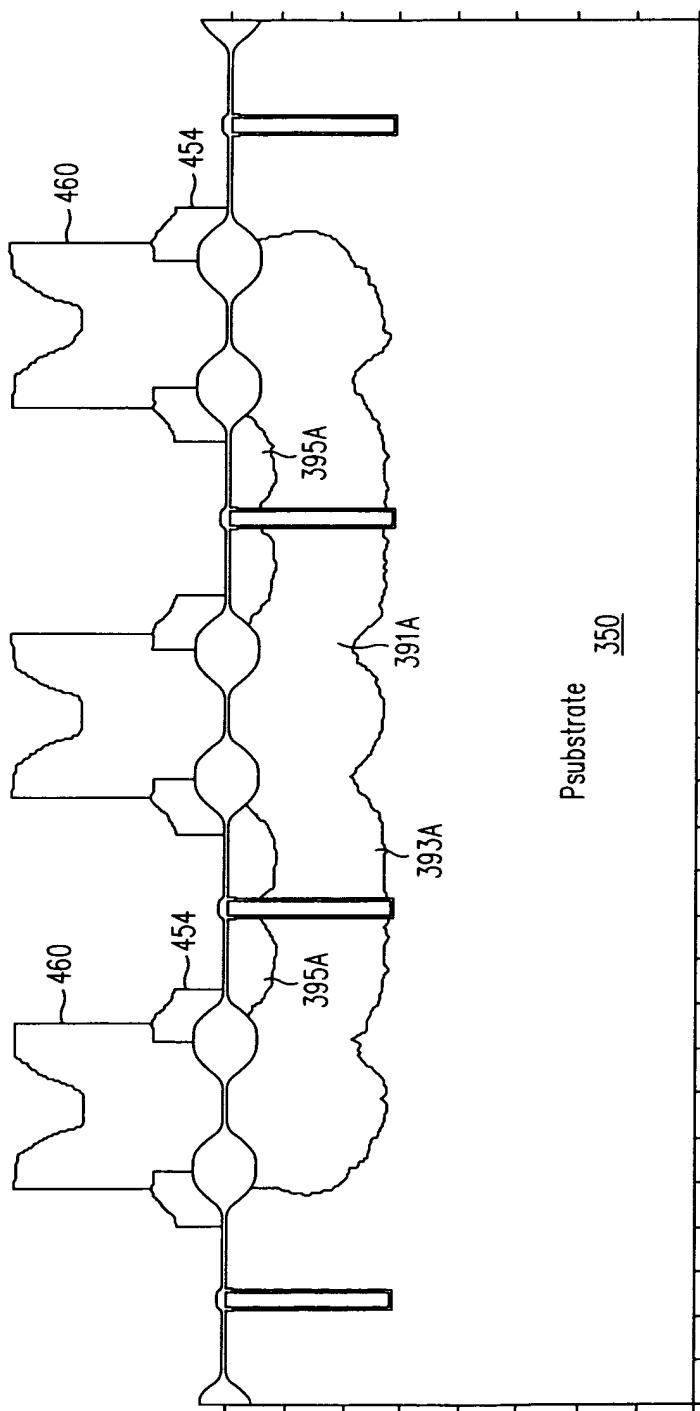


N-Base Mask and Implant

FIG. 54 E



30V Lateral Trench DMOS ~ 308

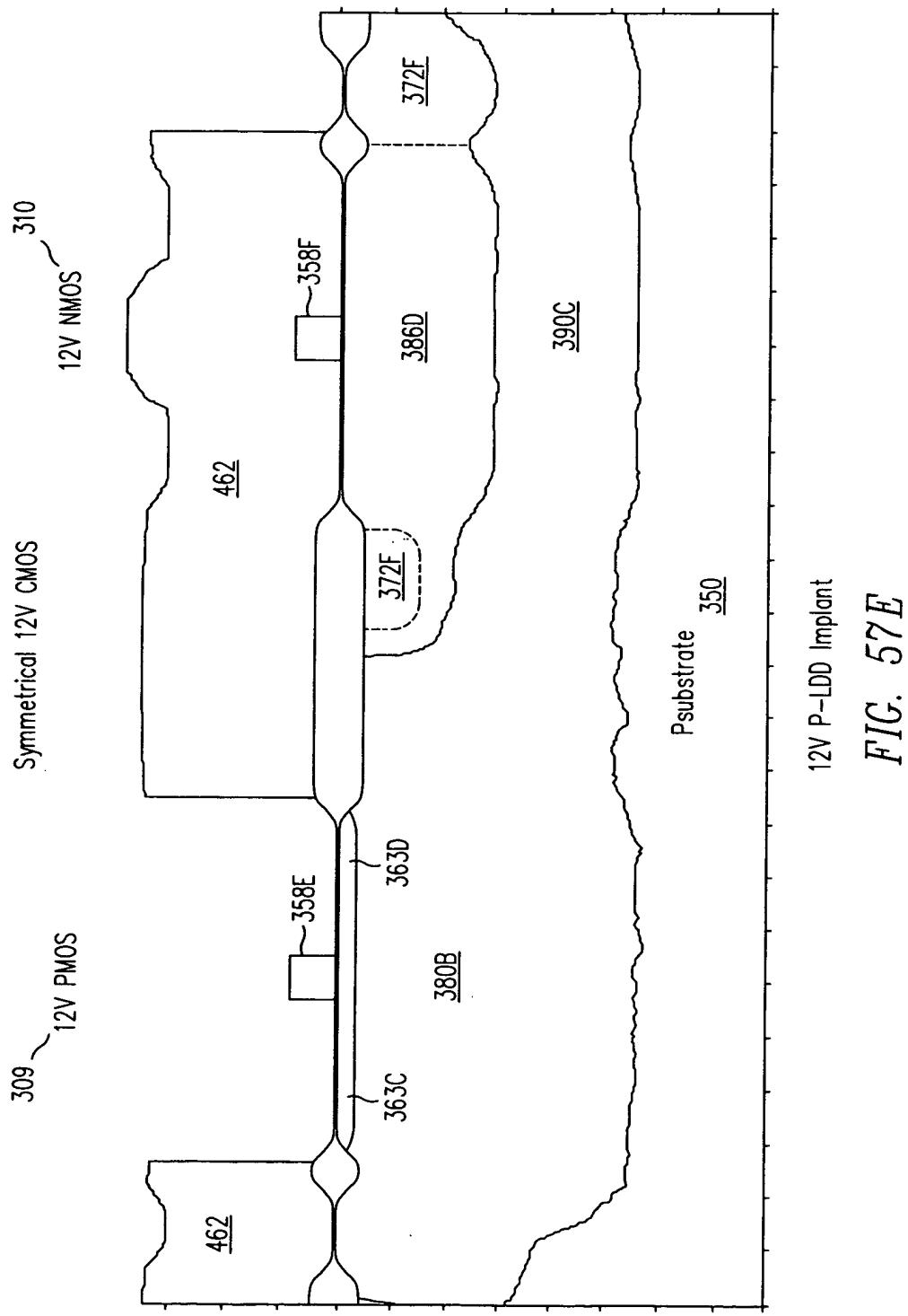


P substrate
350

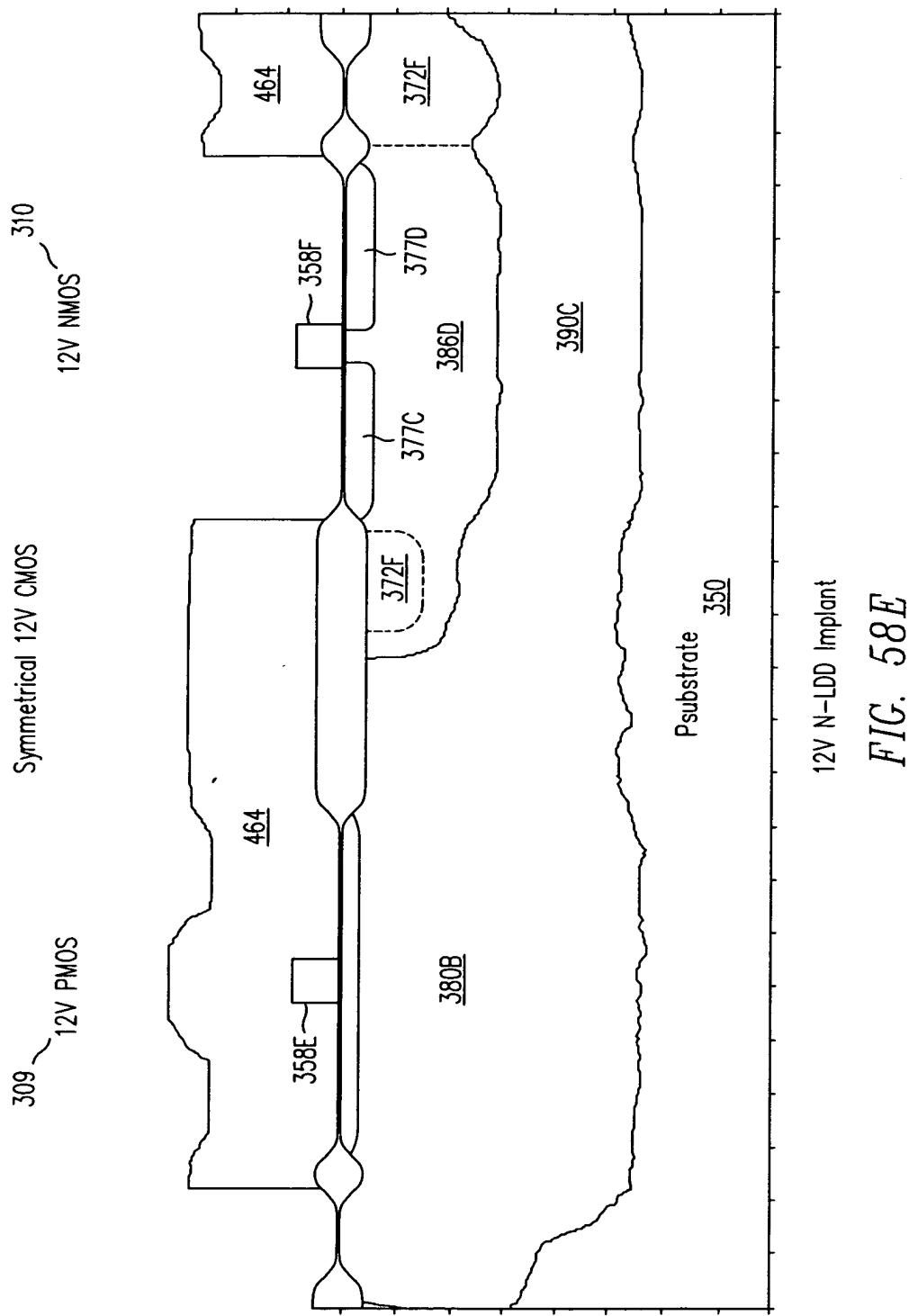
P Body Mask and Implant - Second Stage

FIG. 56D

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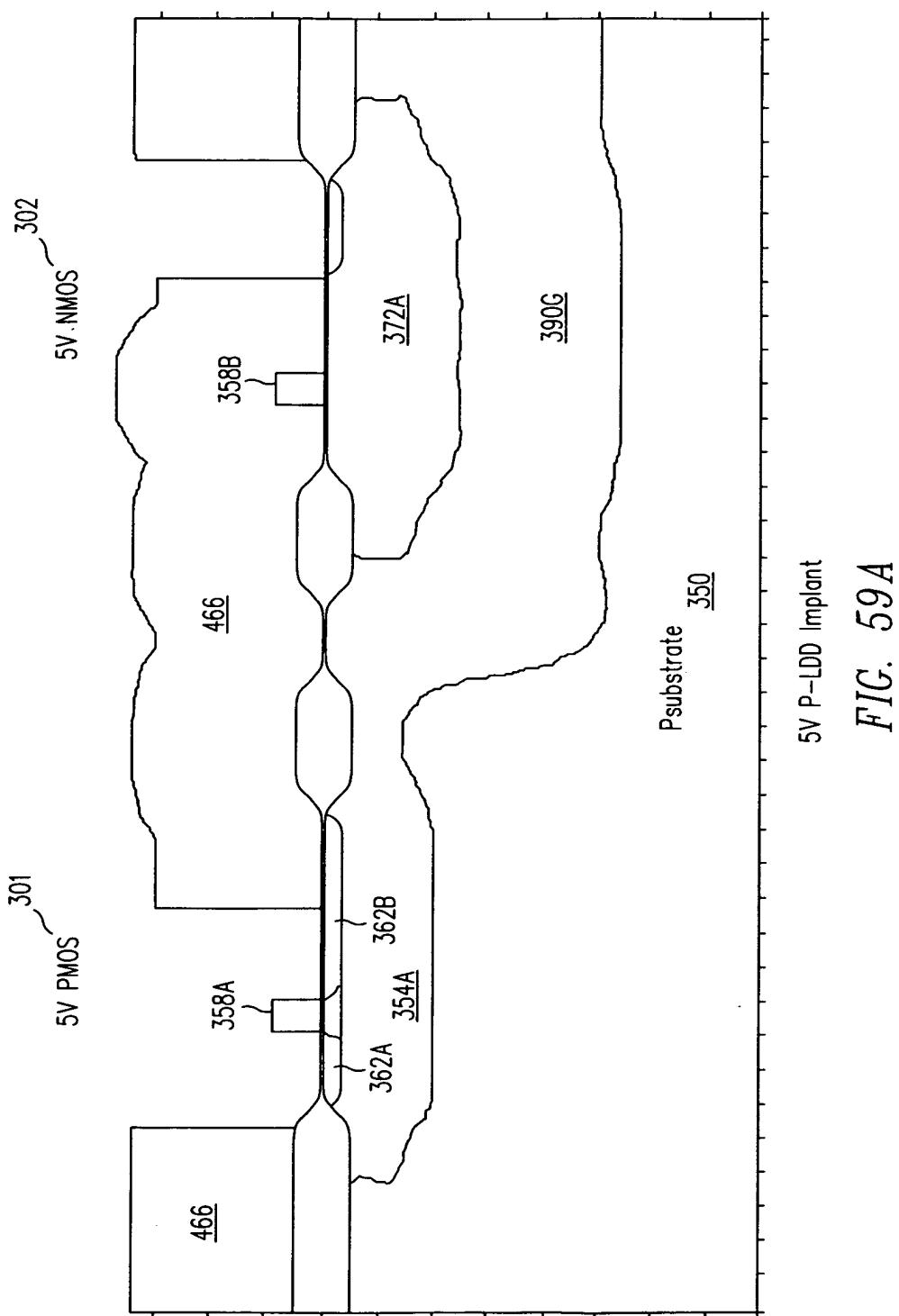
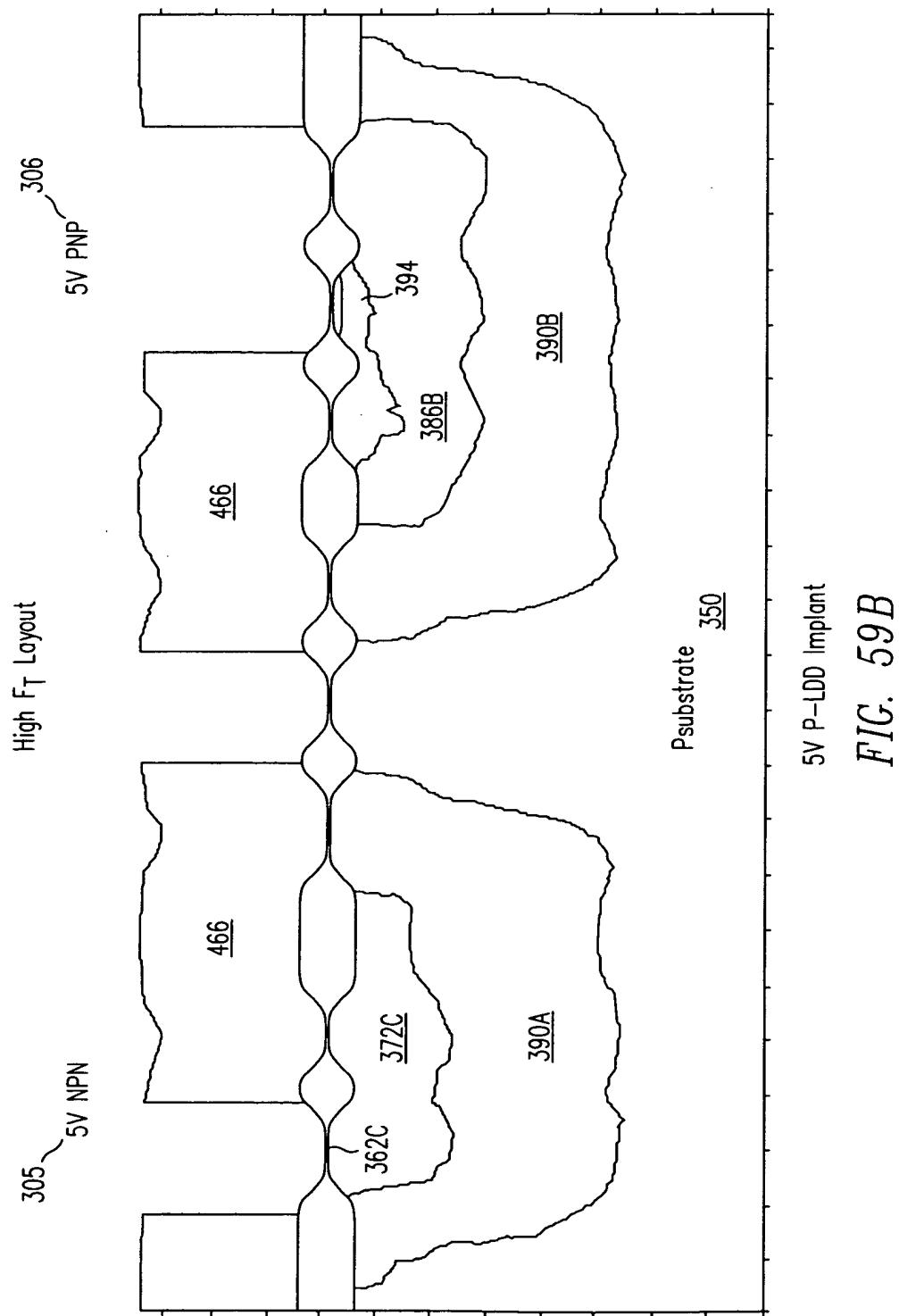
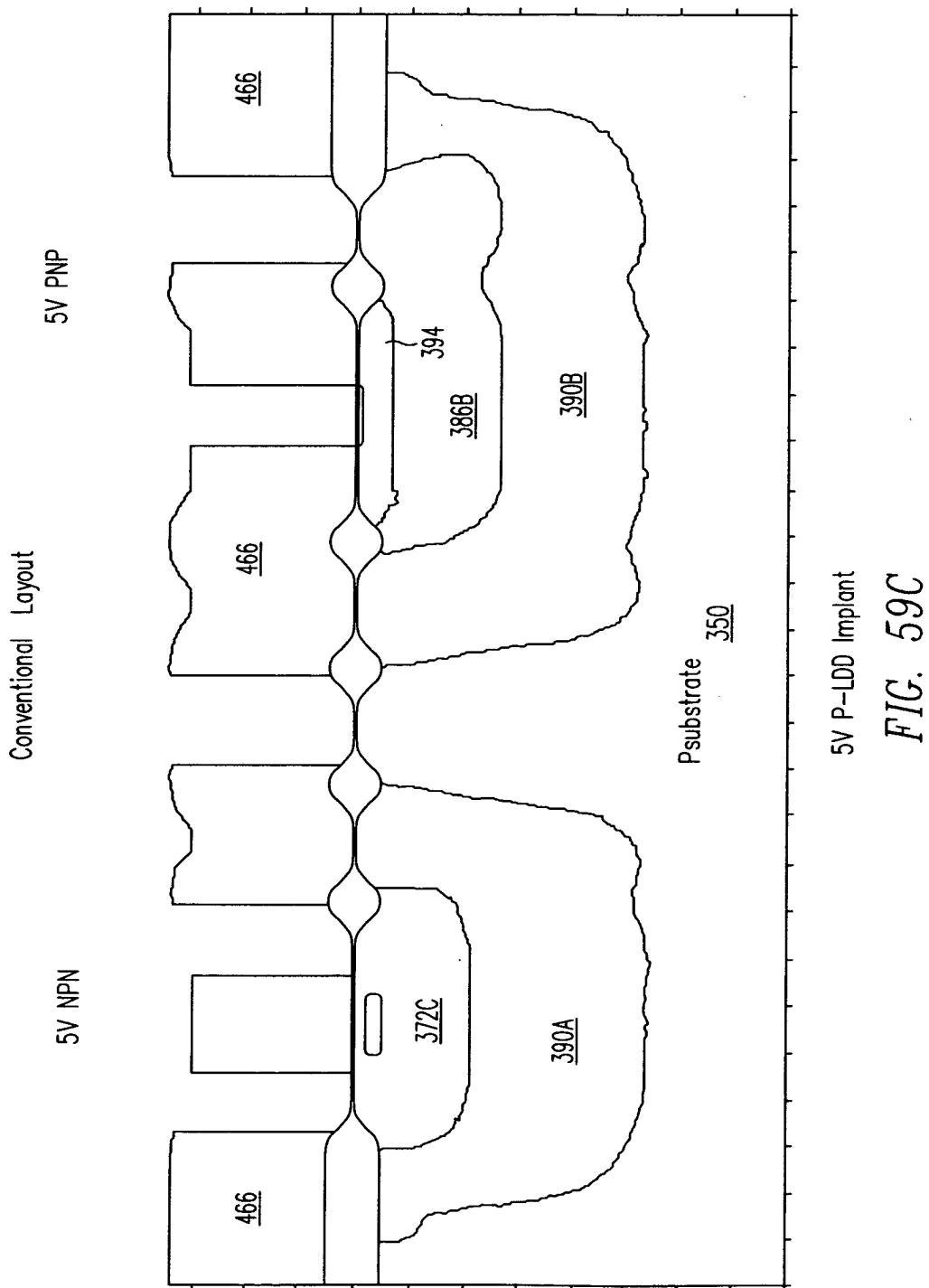
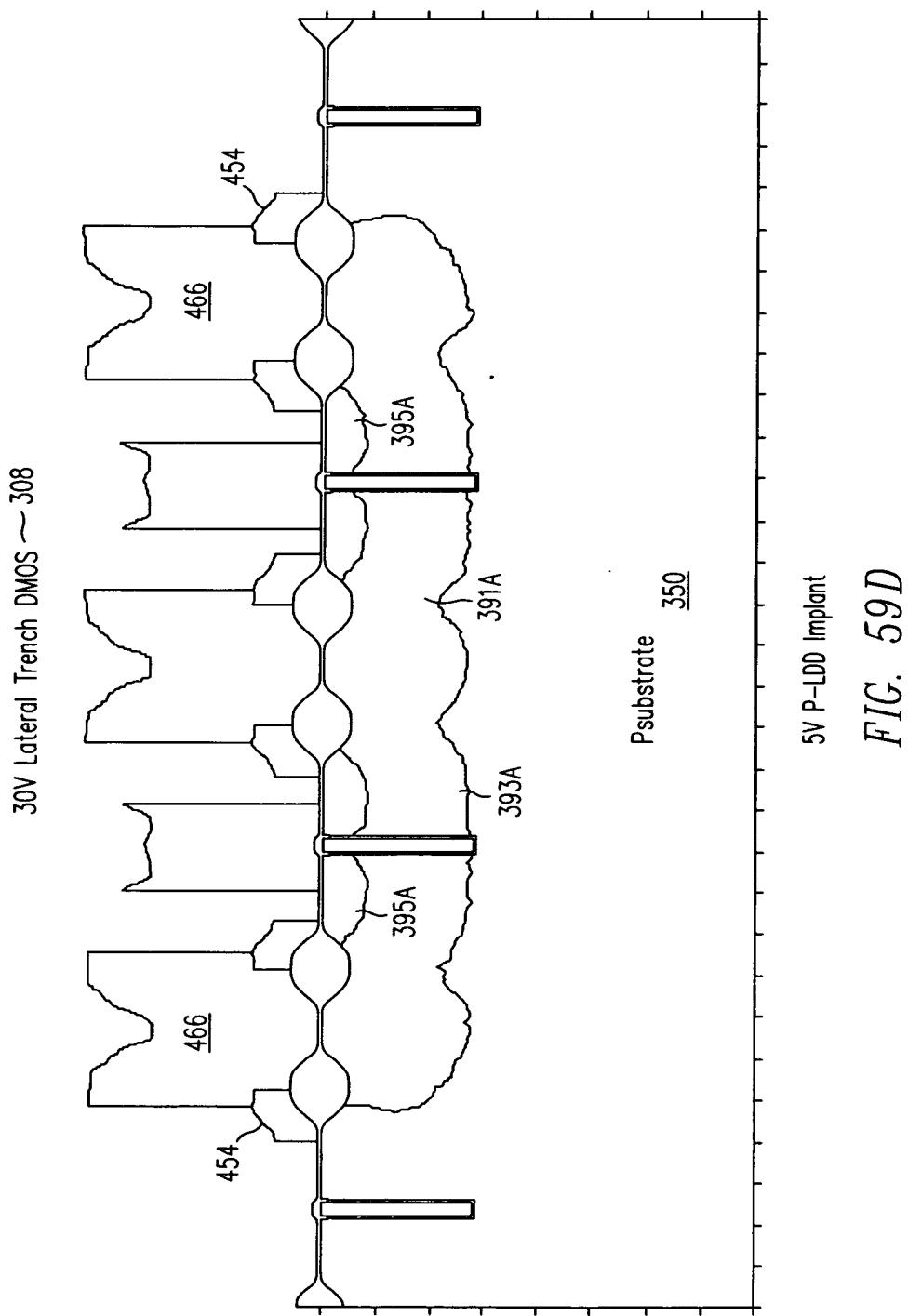


FIG. 59A

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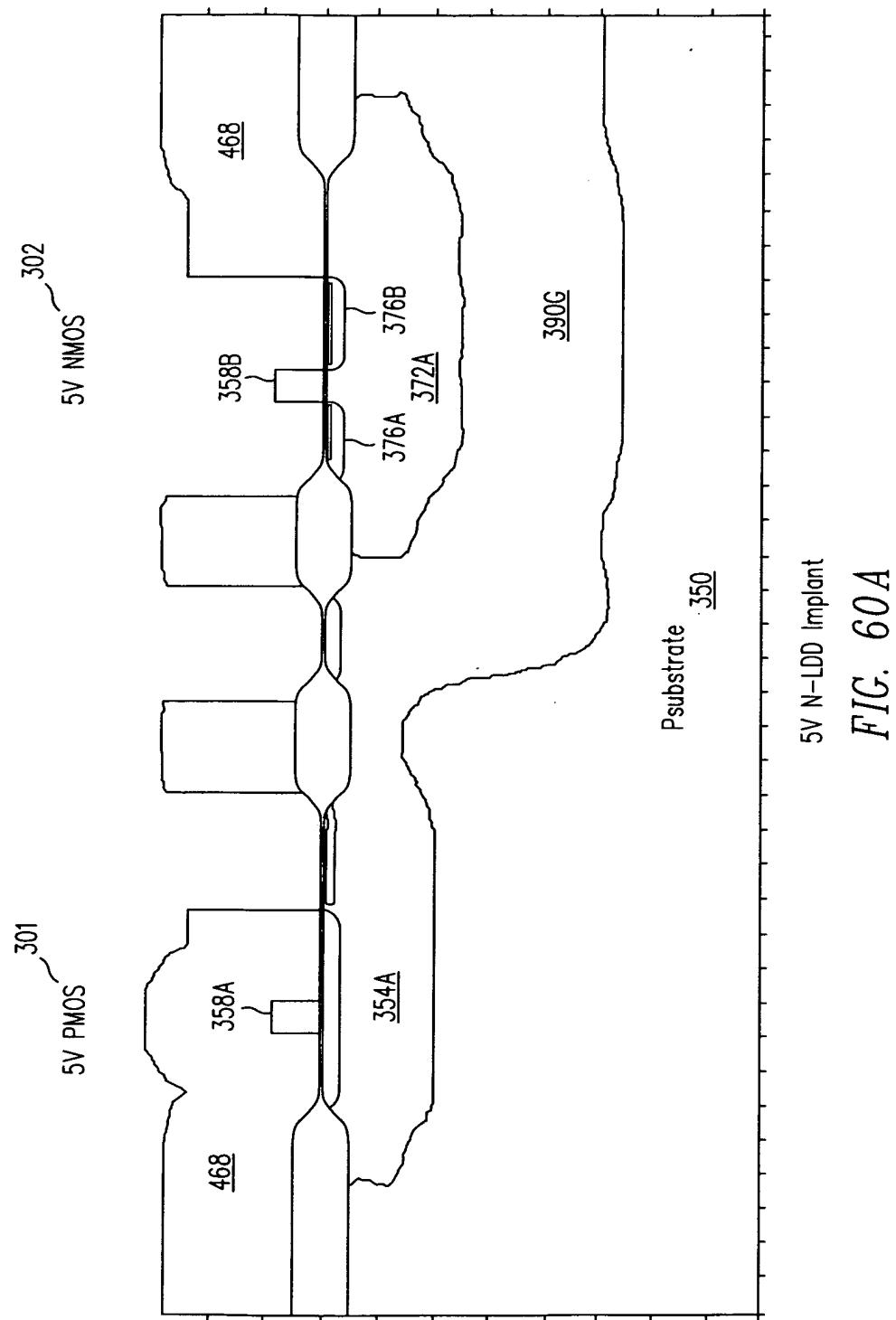


FIG. 60A

5V N-LDD implant

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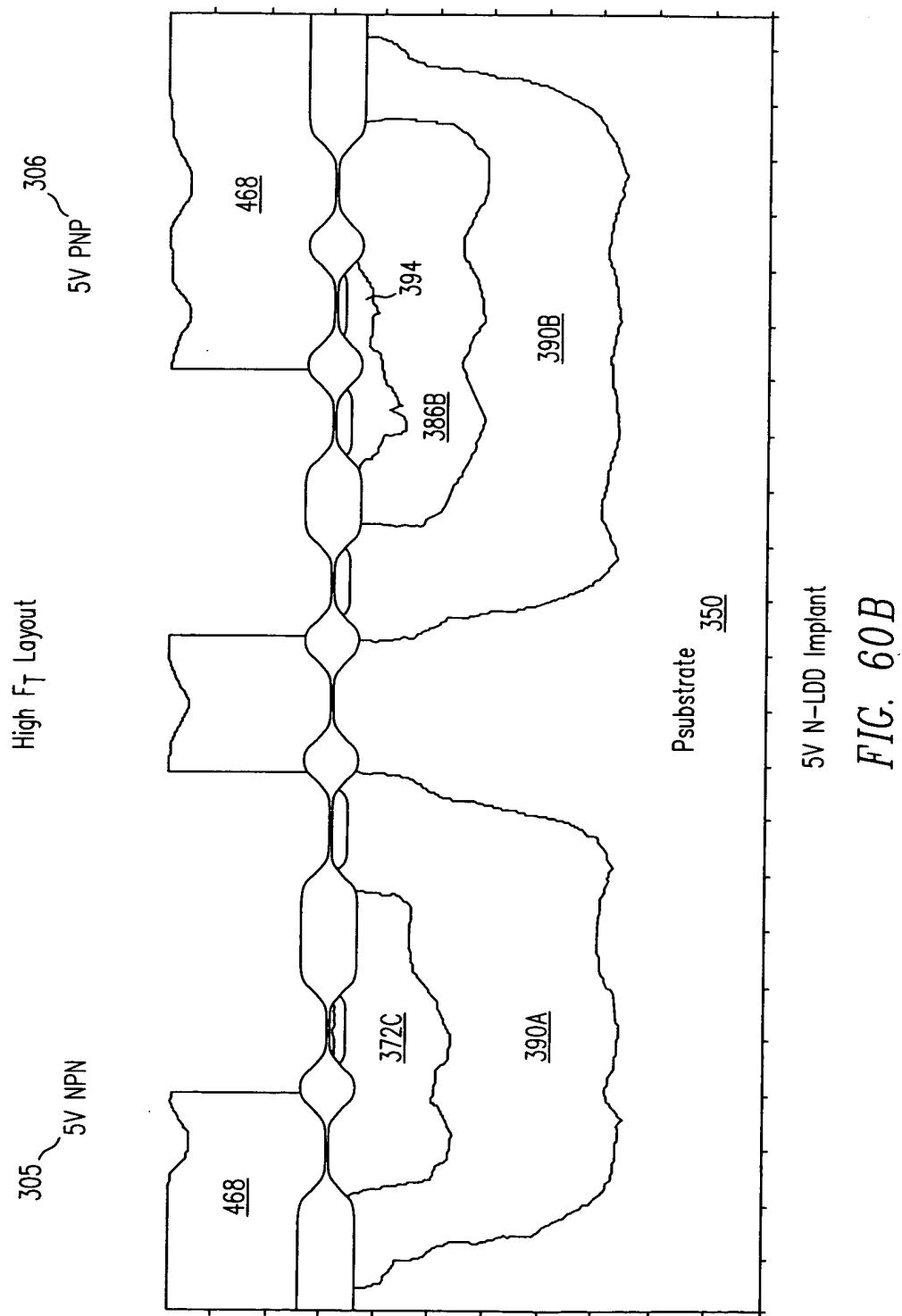
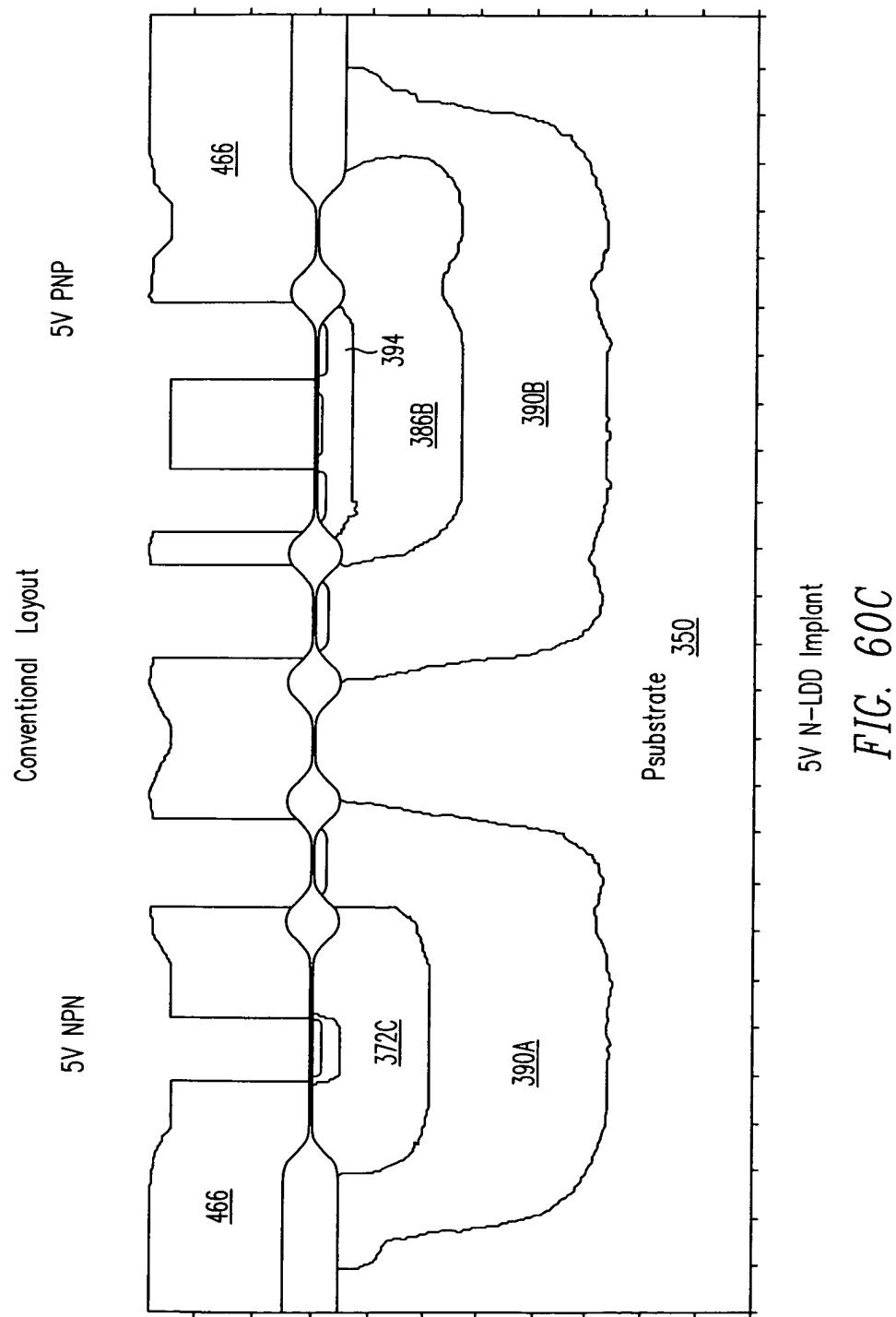
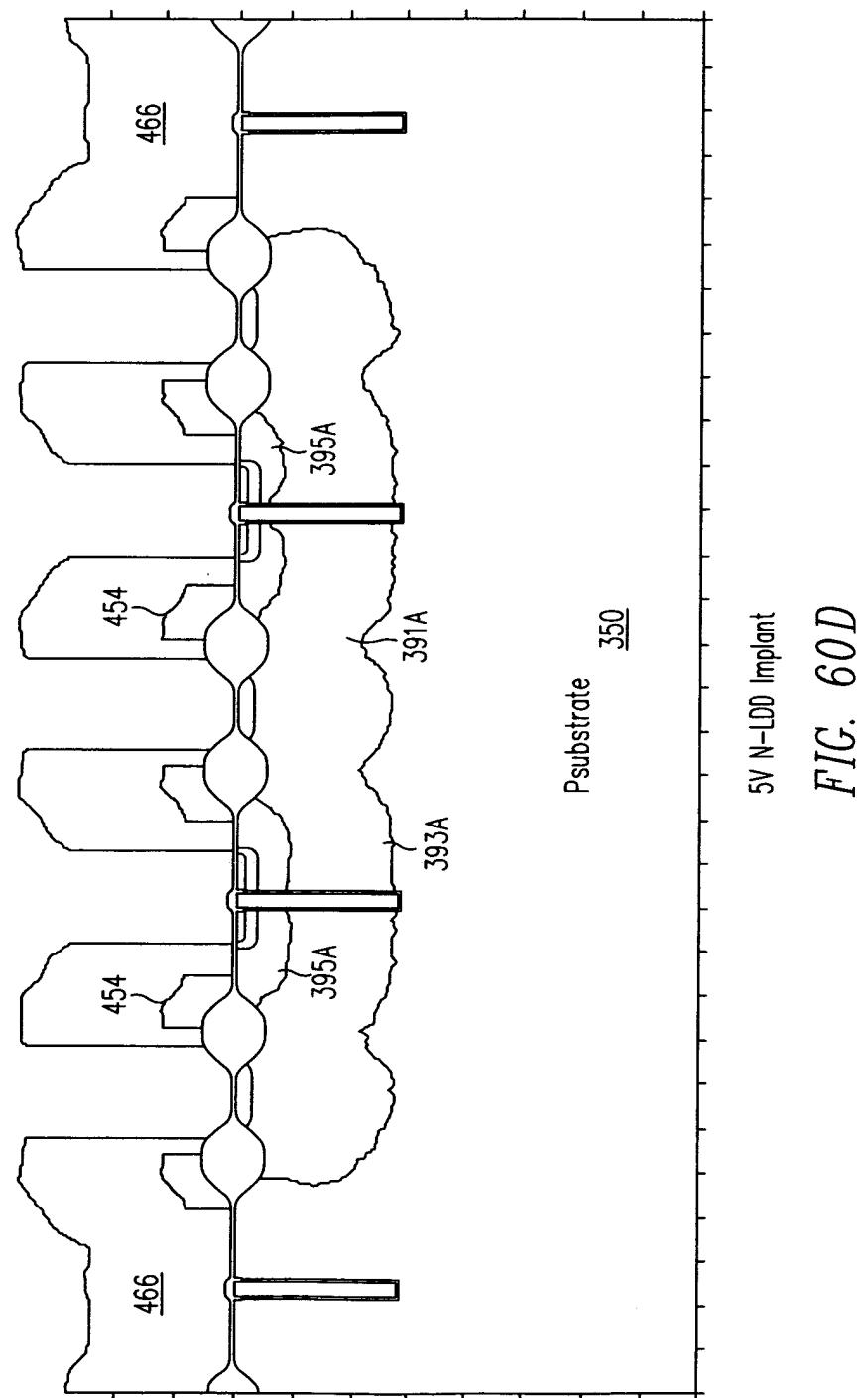


FIG. 60B



30V Lateral Trench DMOS ~ 308



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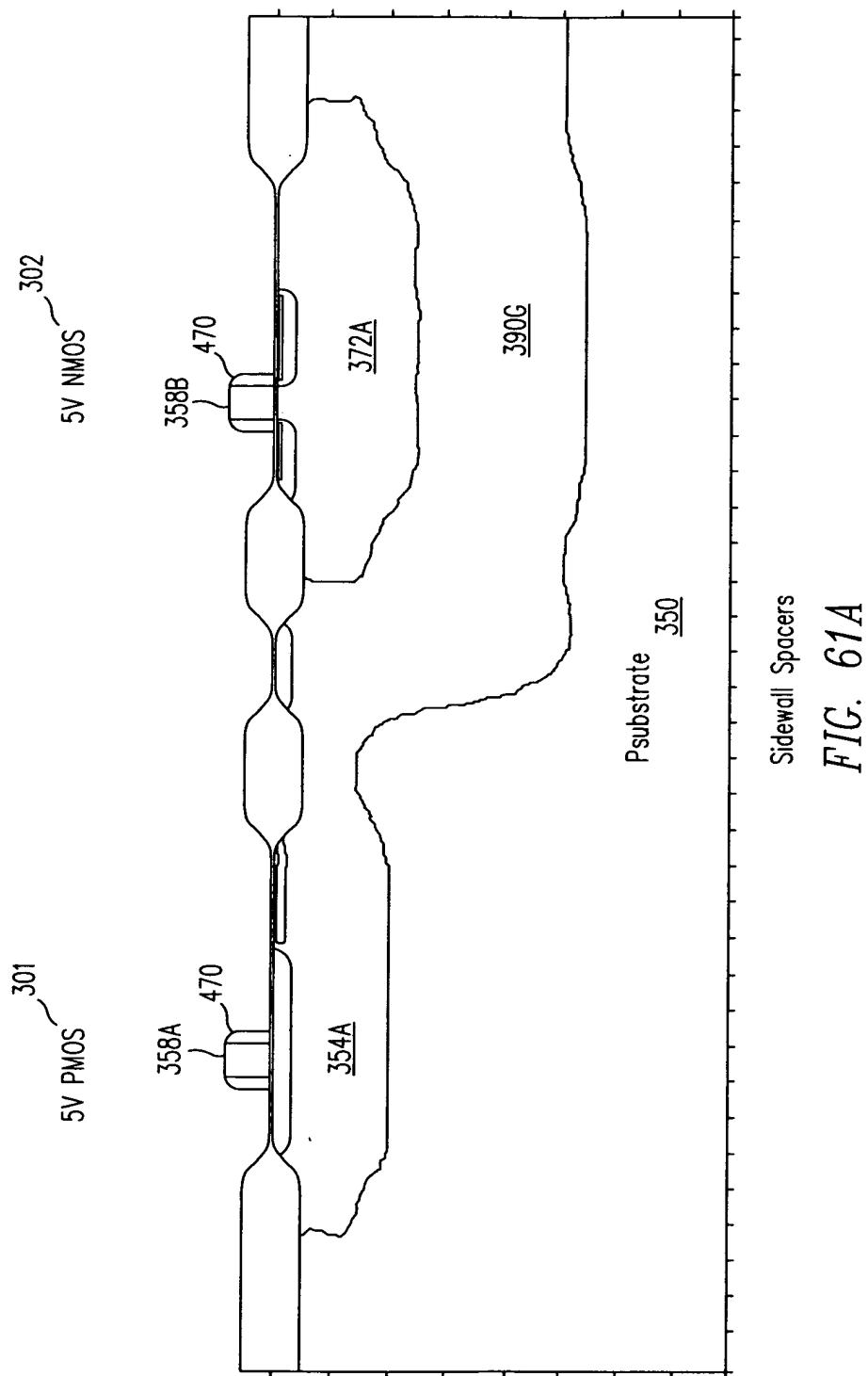
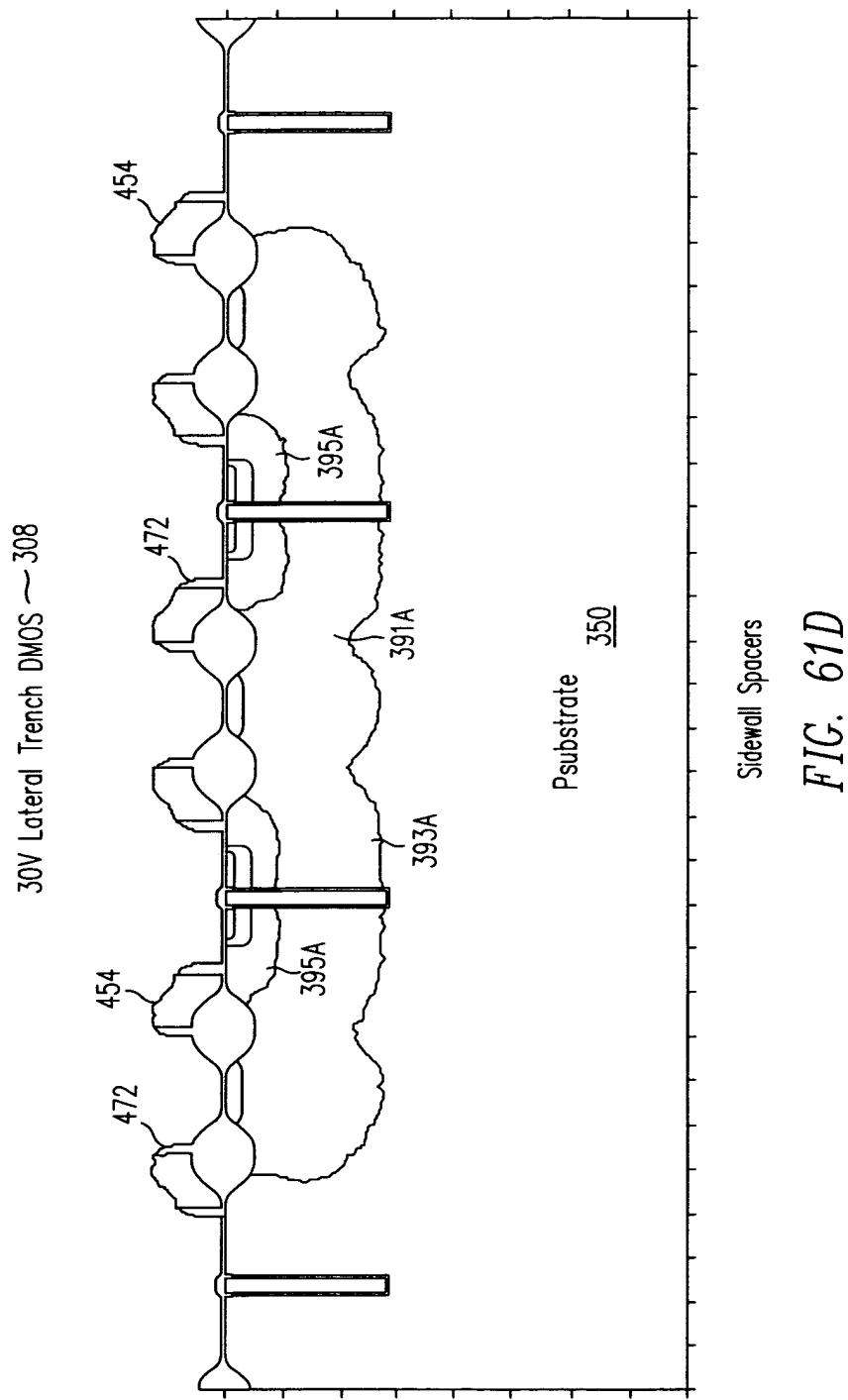


FIG. 61A

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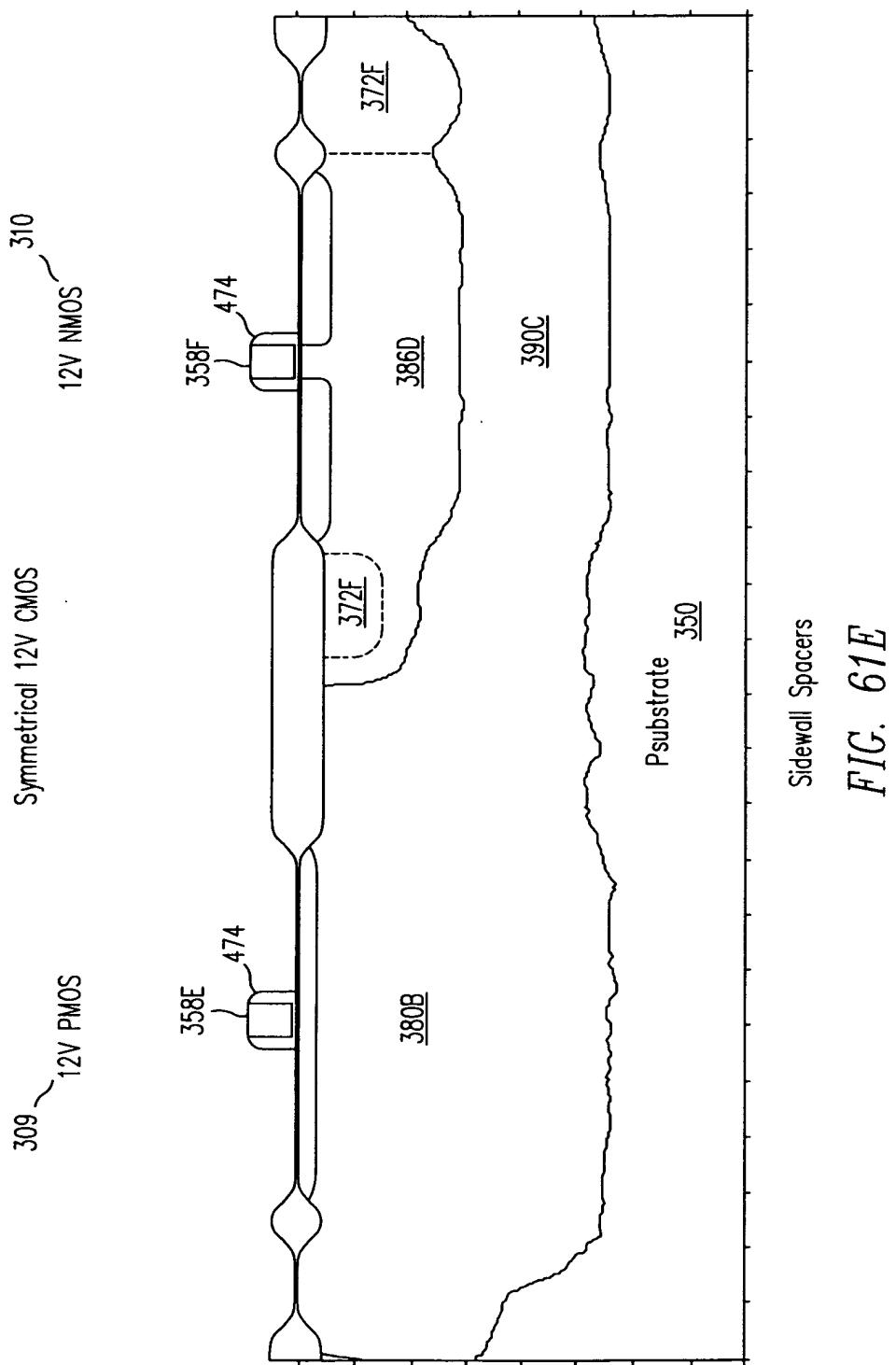


FIG. 61E

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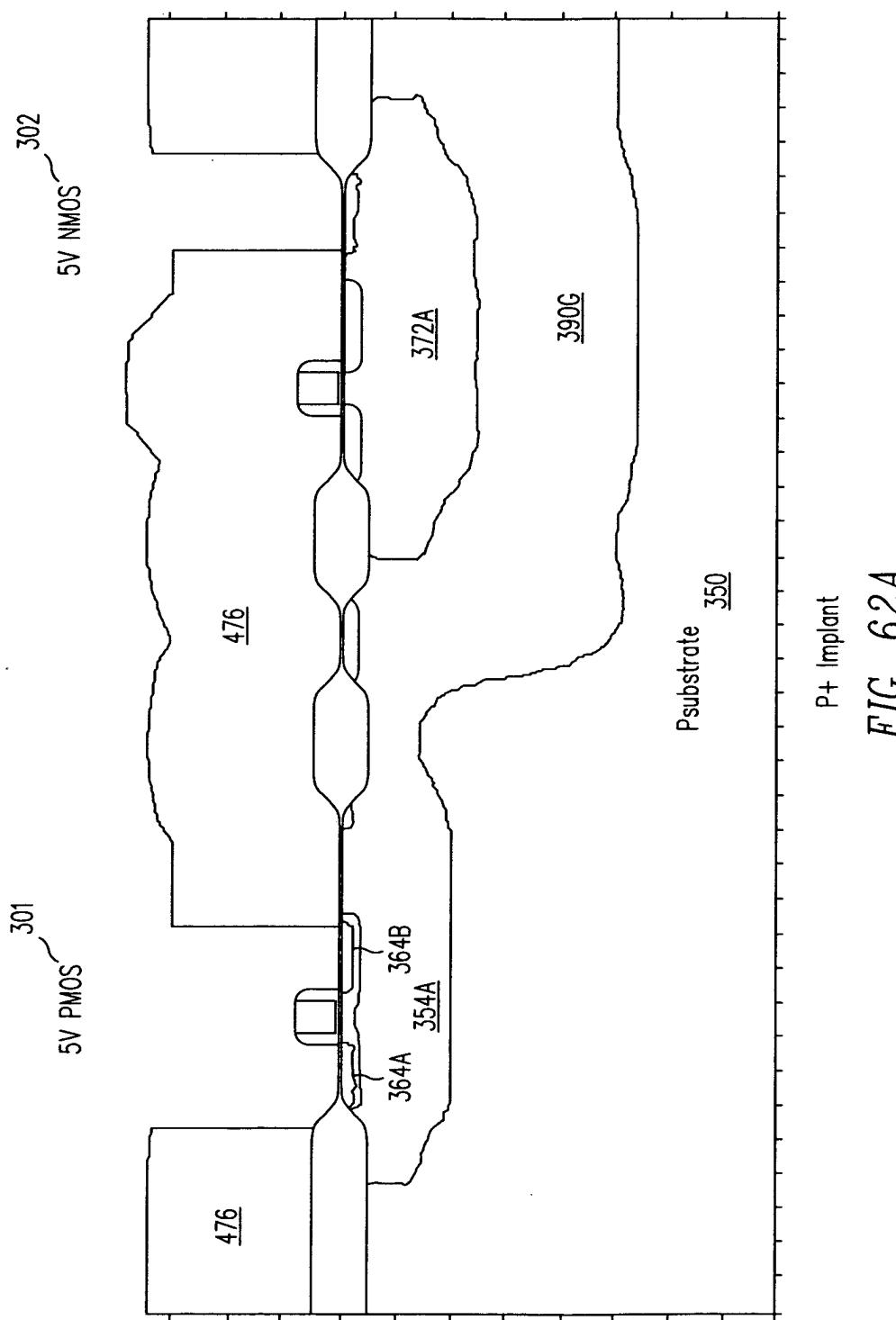
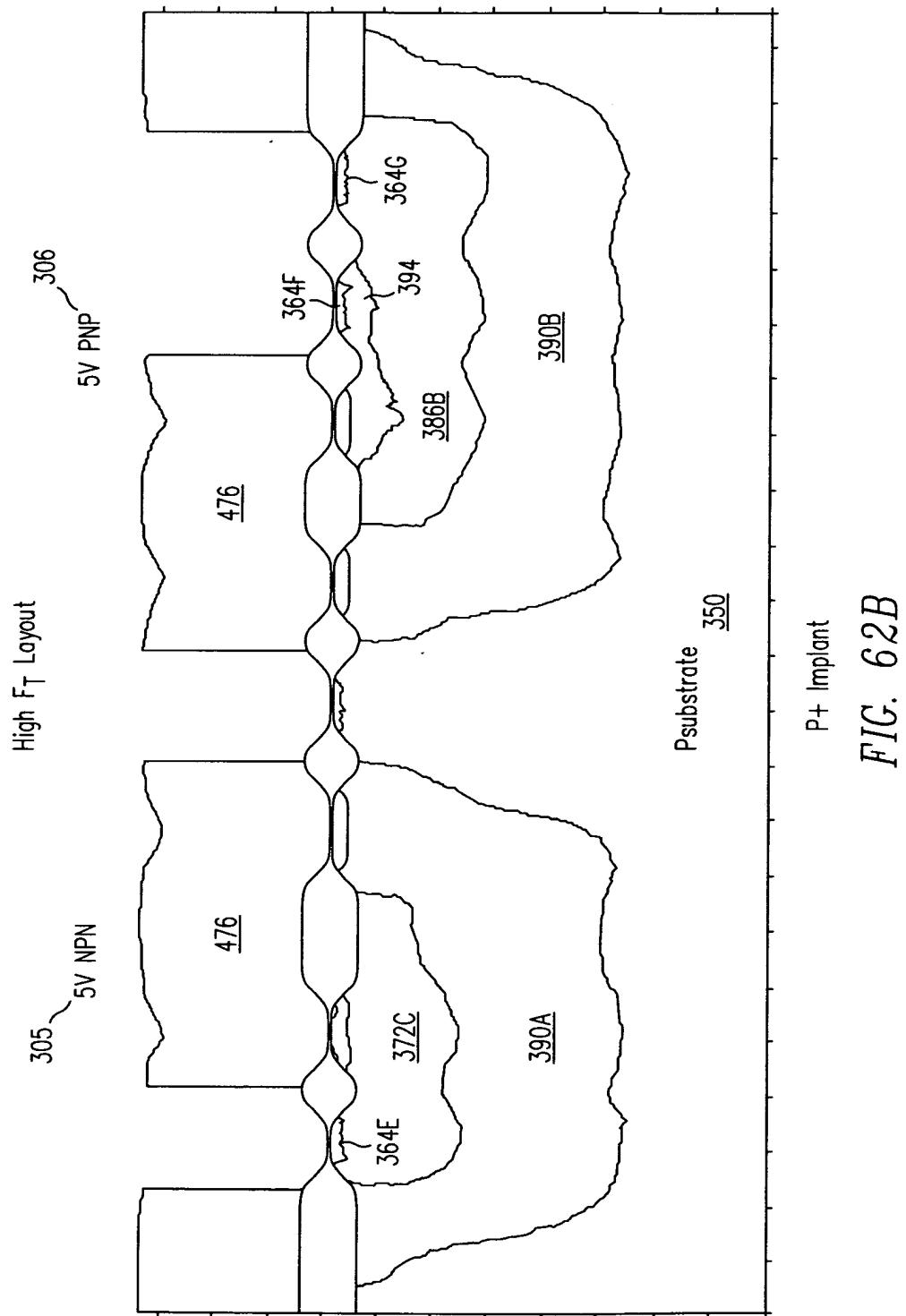
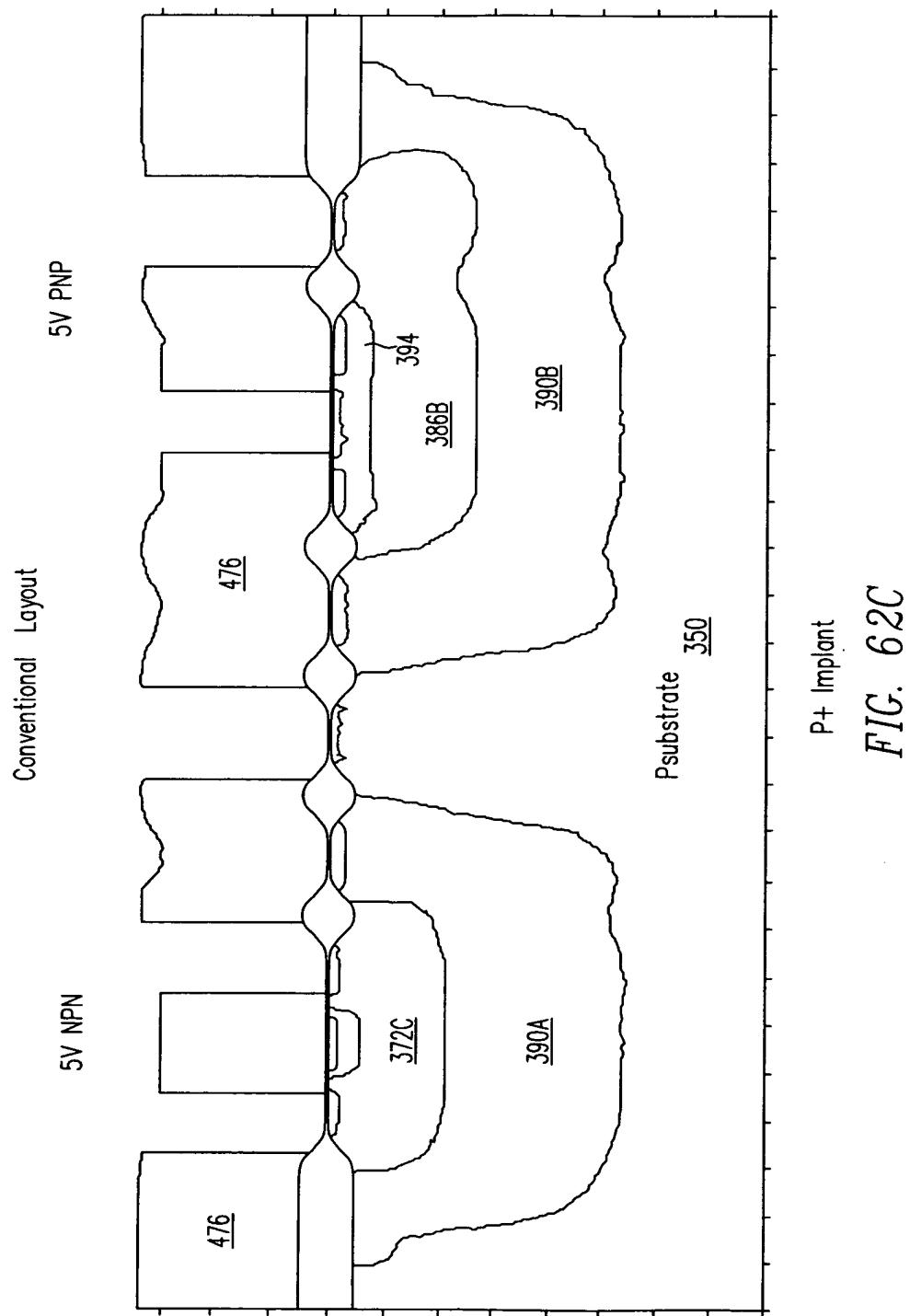


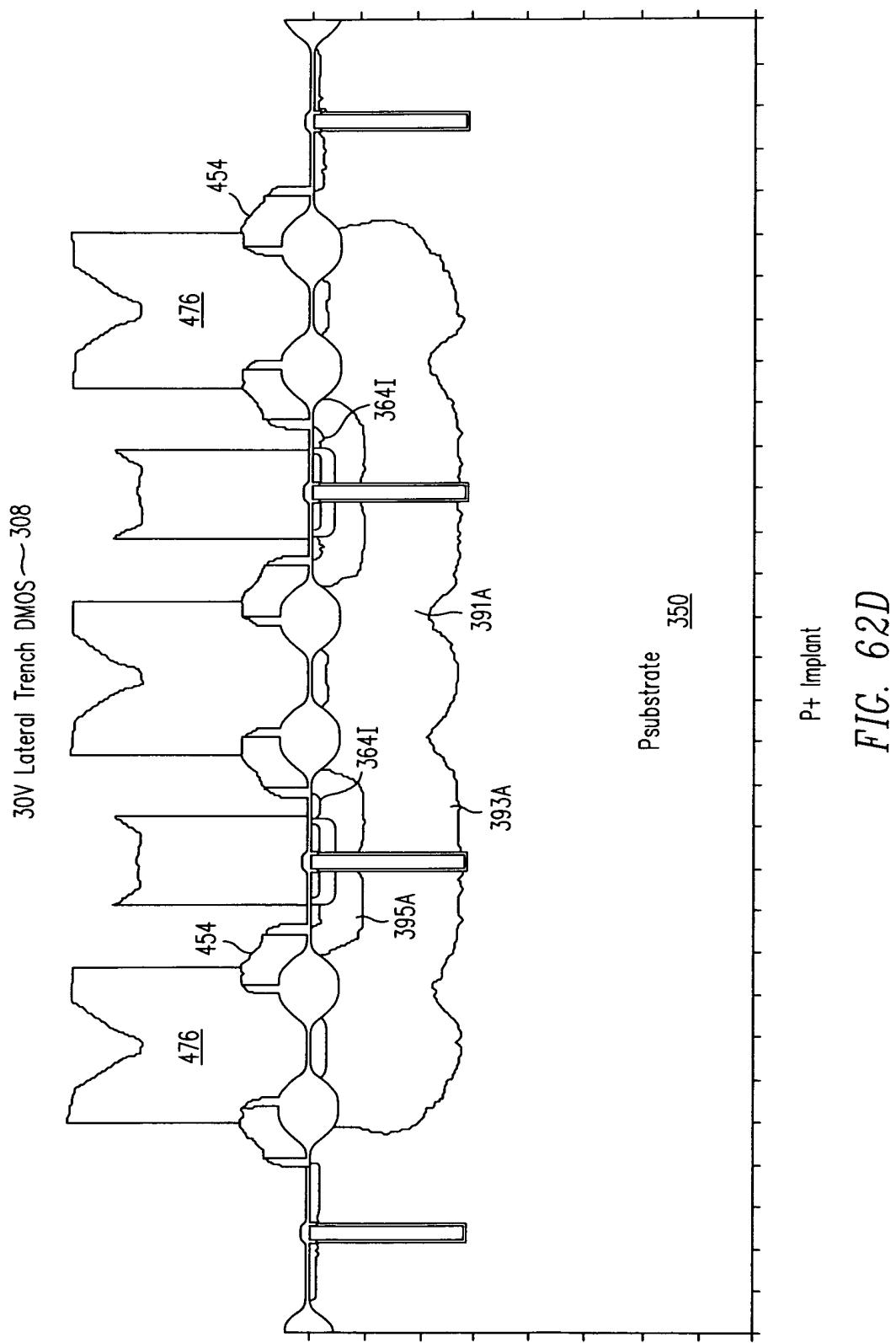
FIG. 62A



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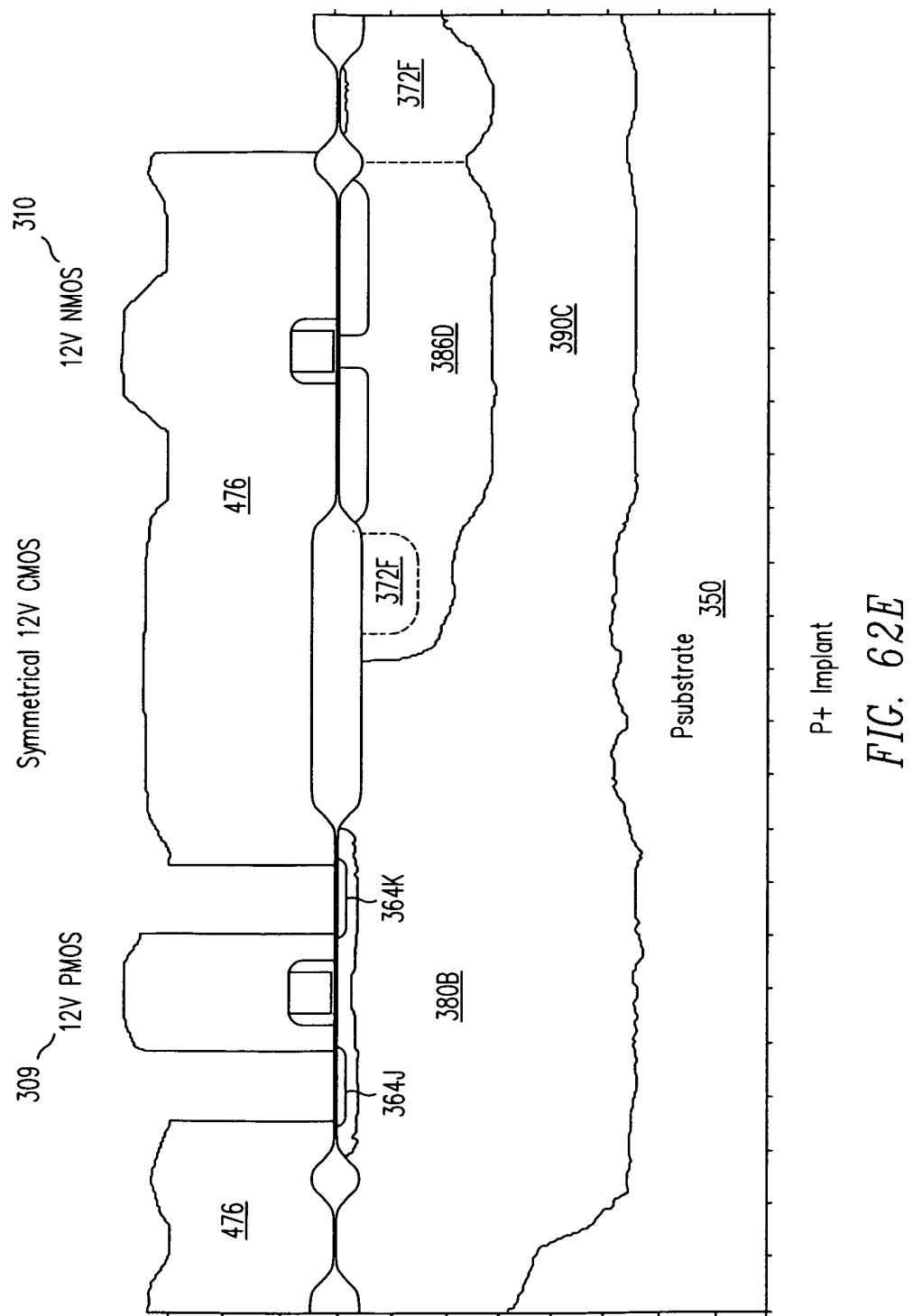


FIG. 62E

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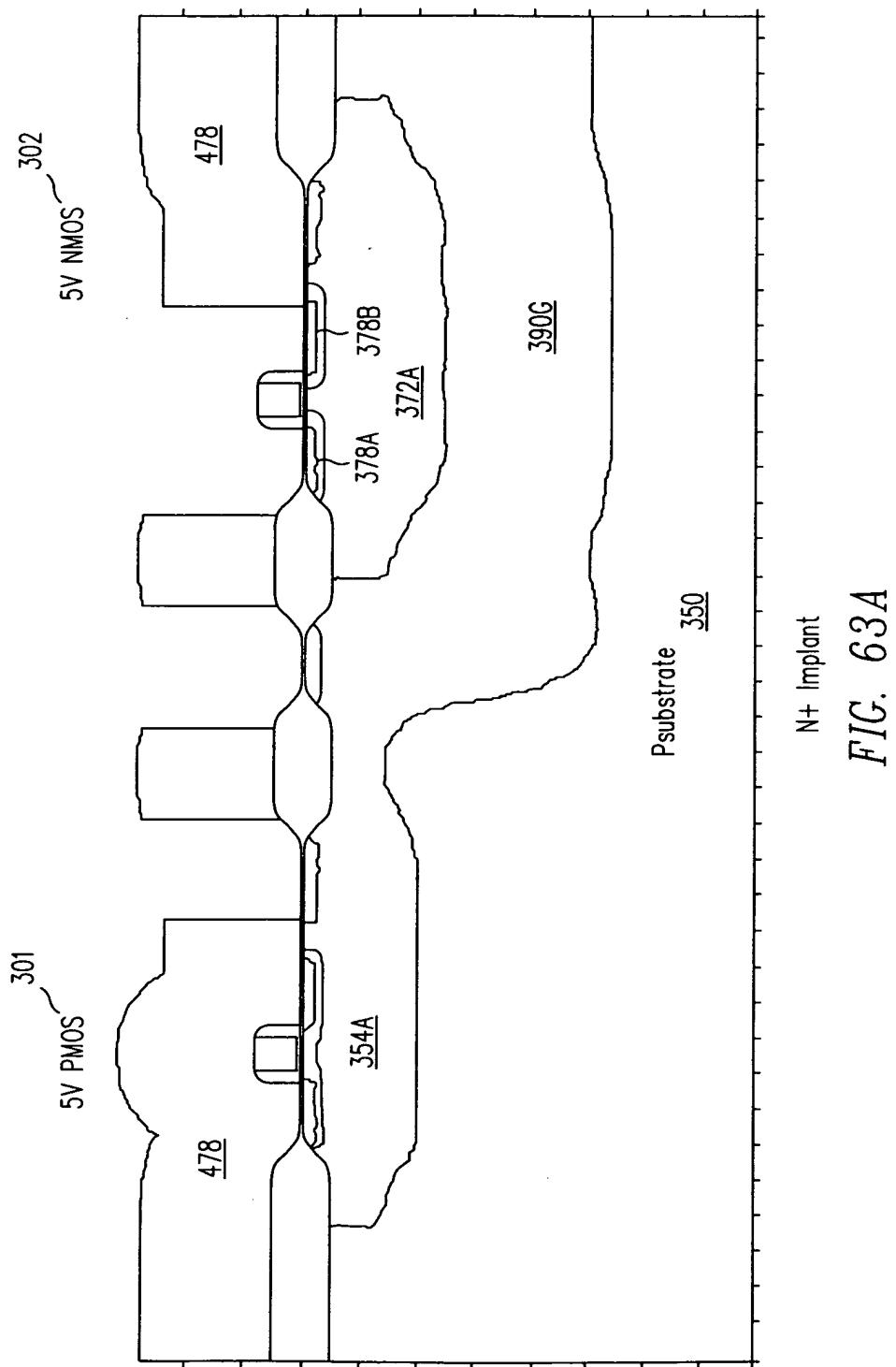
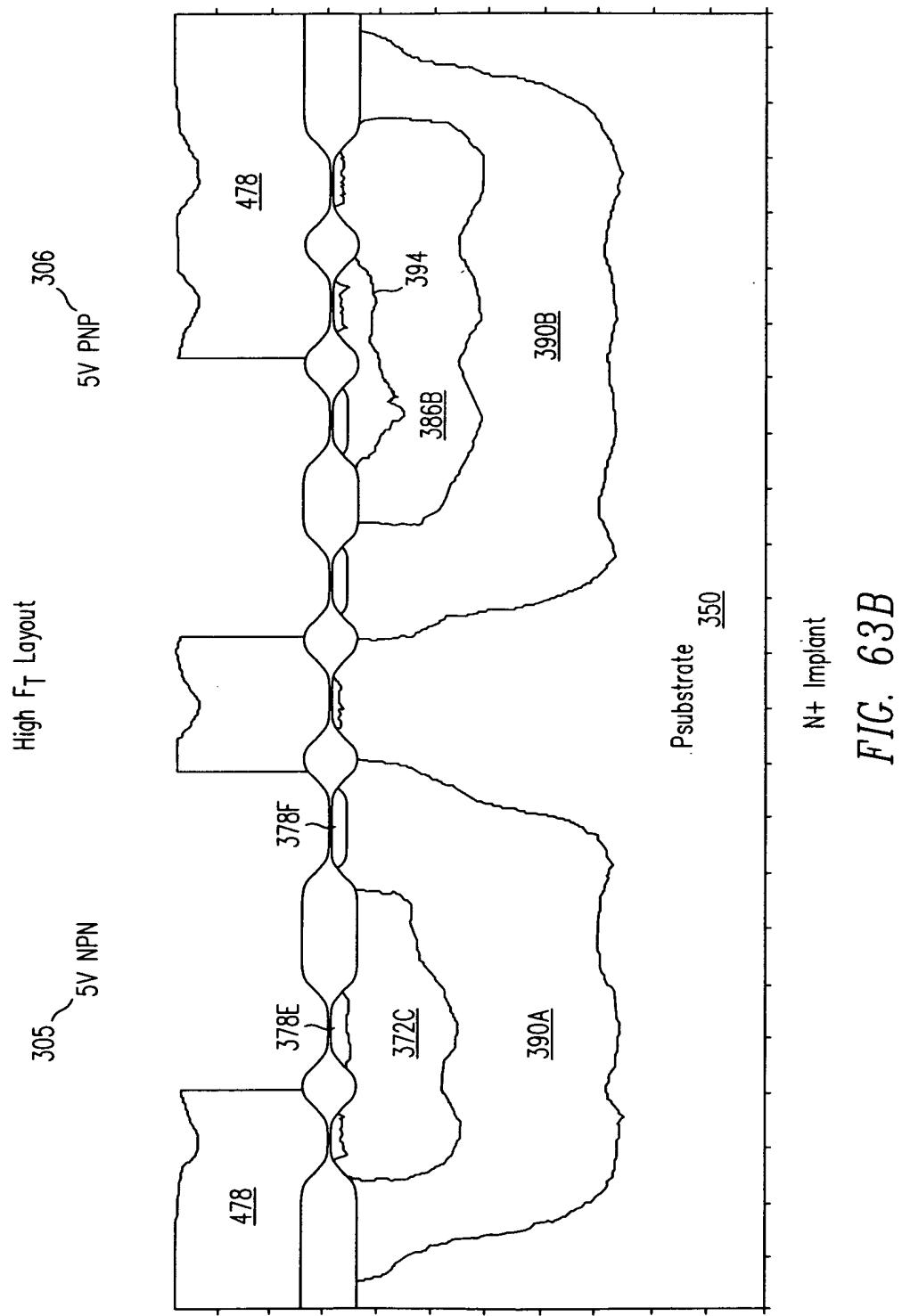


FIG. 63A

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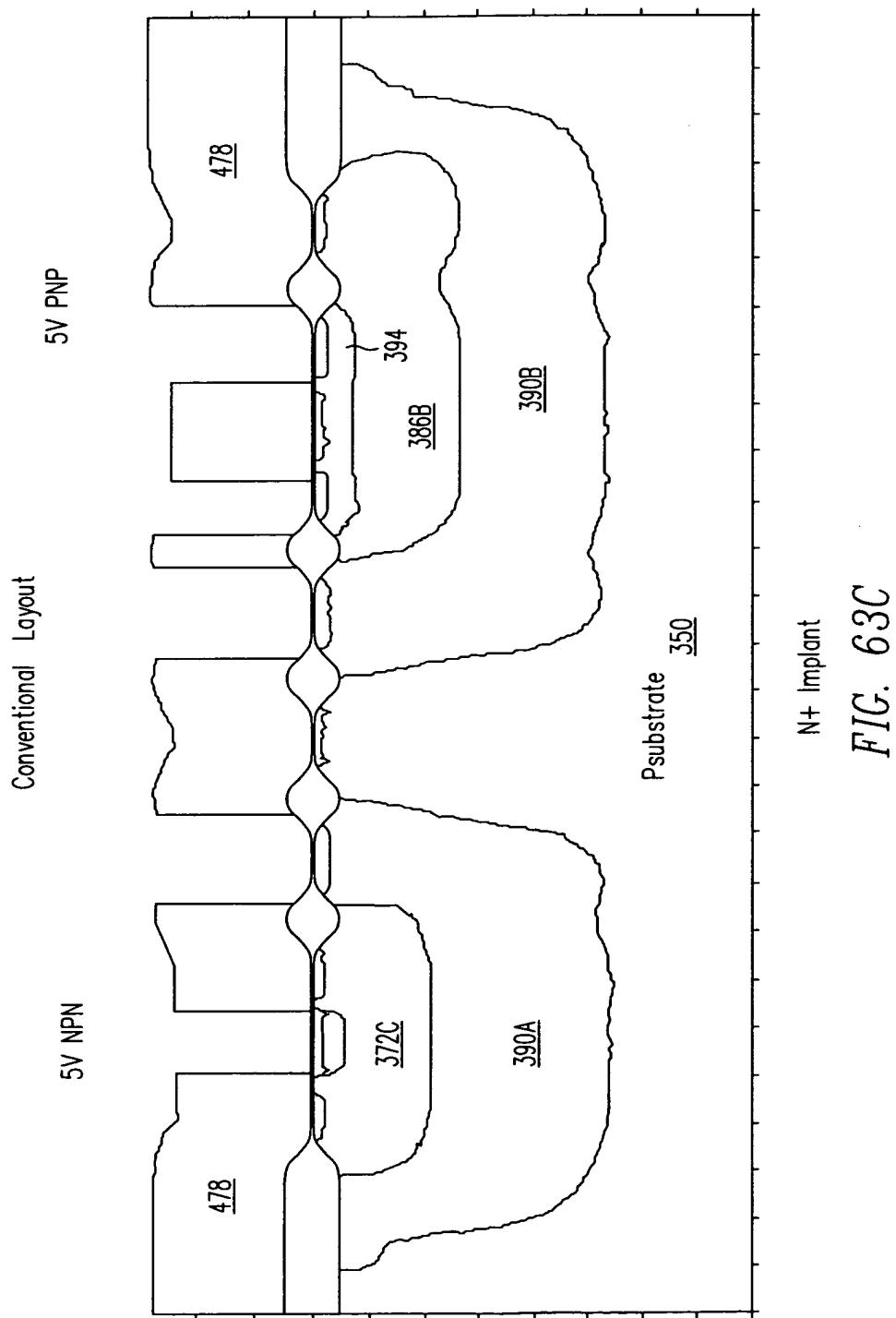


FIG. 63C

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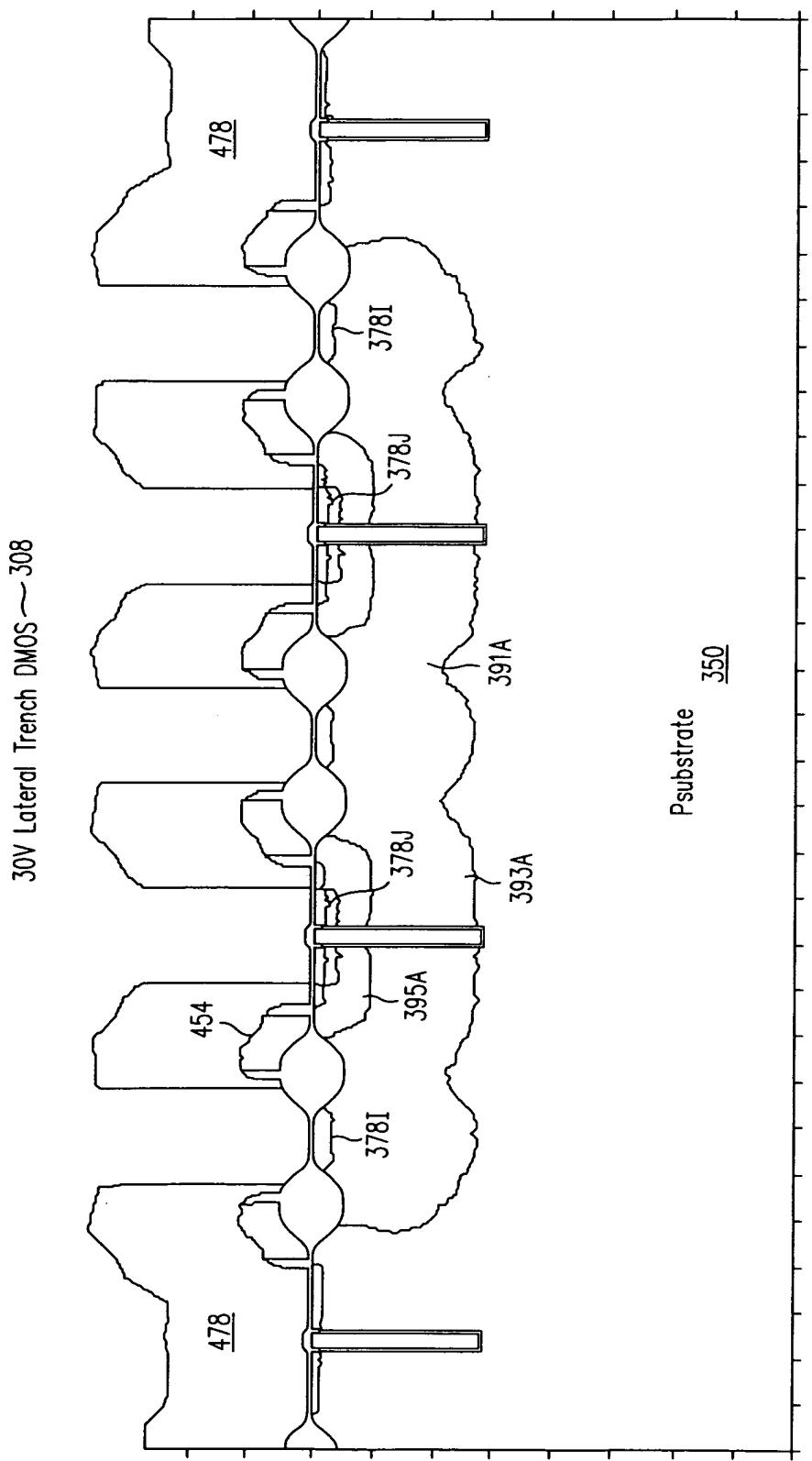


FIG. 63D

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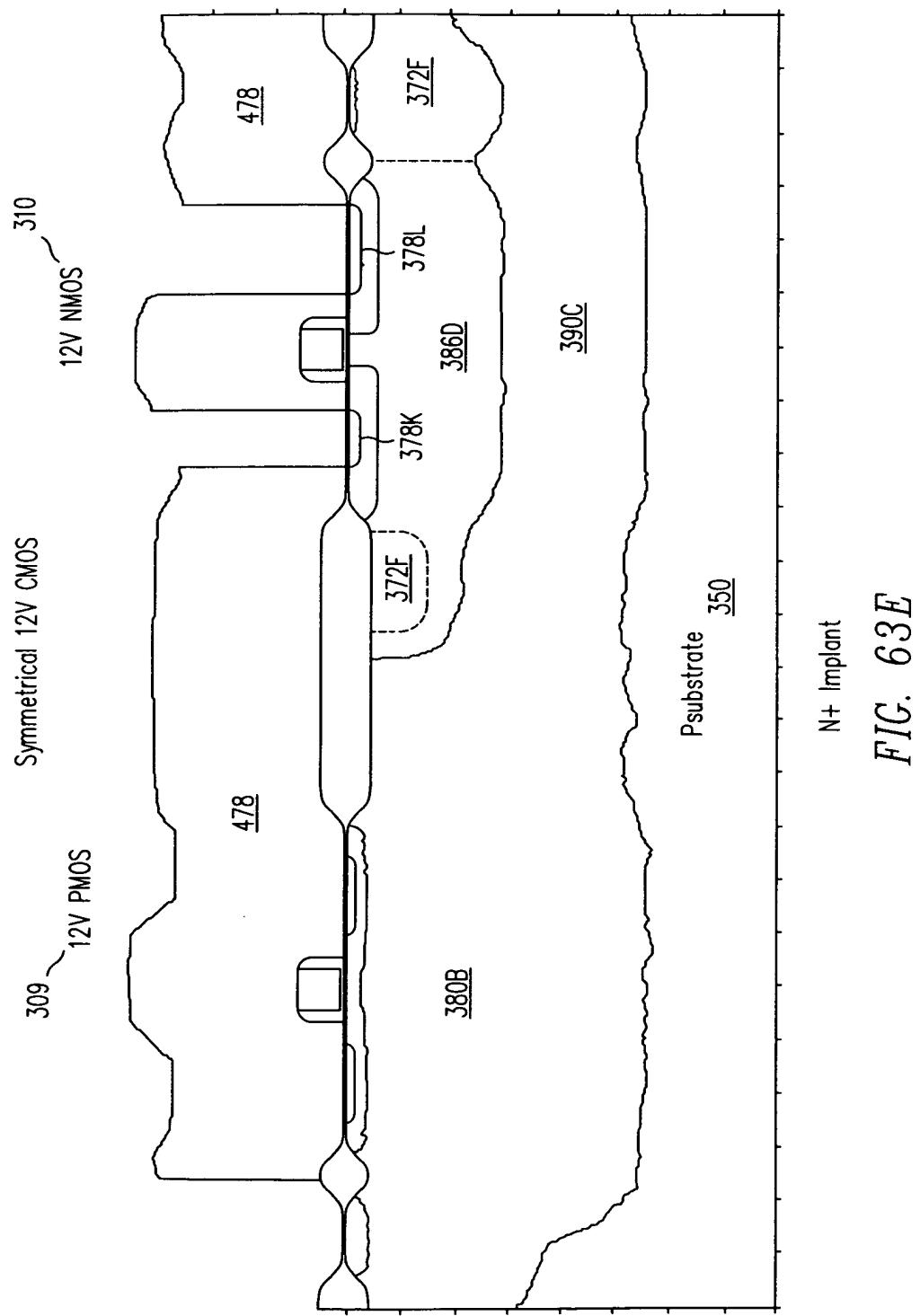
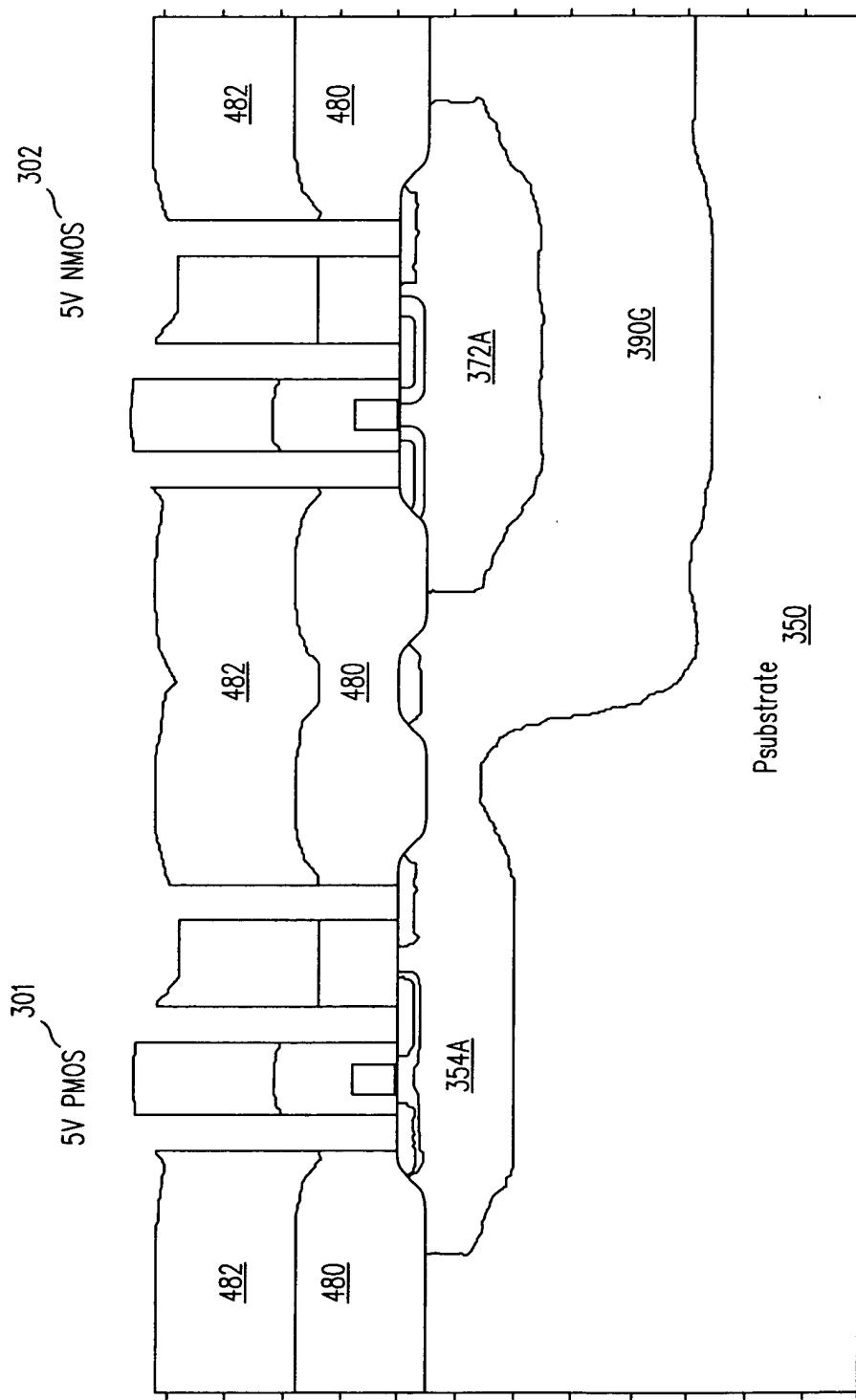


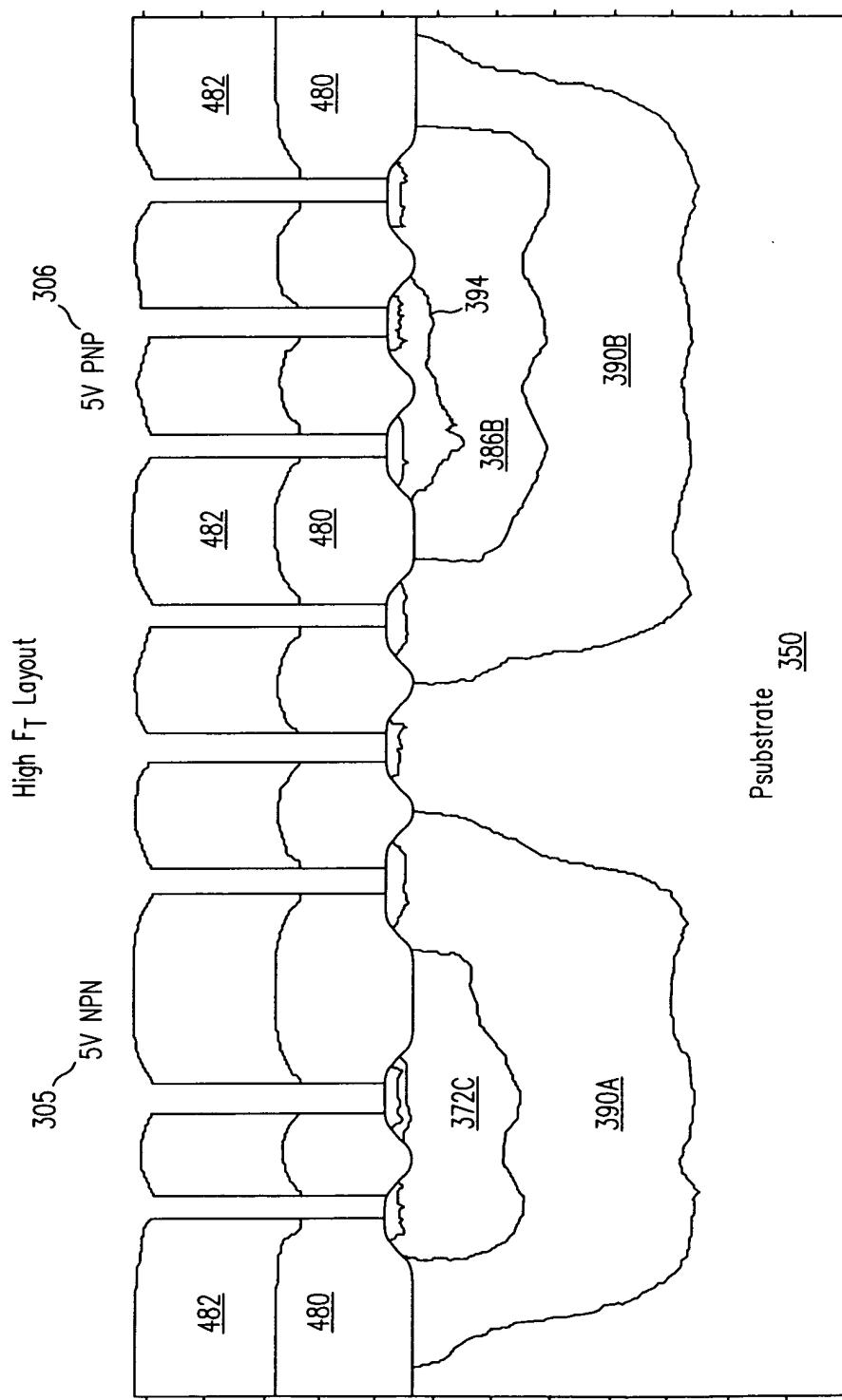
FIG. 63E

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Interlayer Dielectric Deposition and Etch

FIG. 64 A



Interlayer Dielectric Deposition and Etch

FIG. 64B

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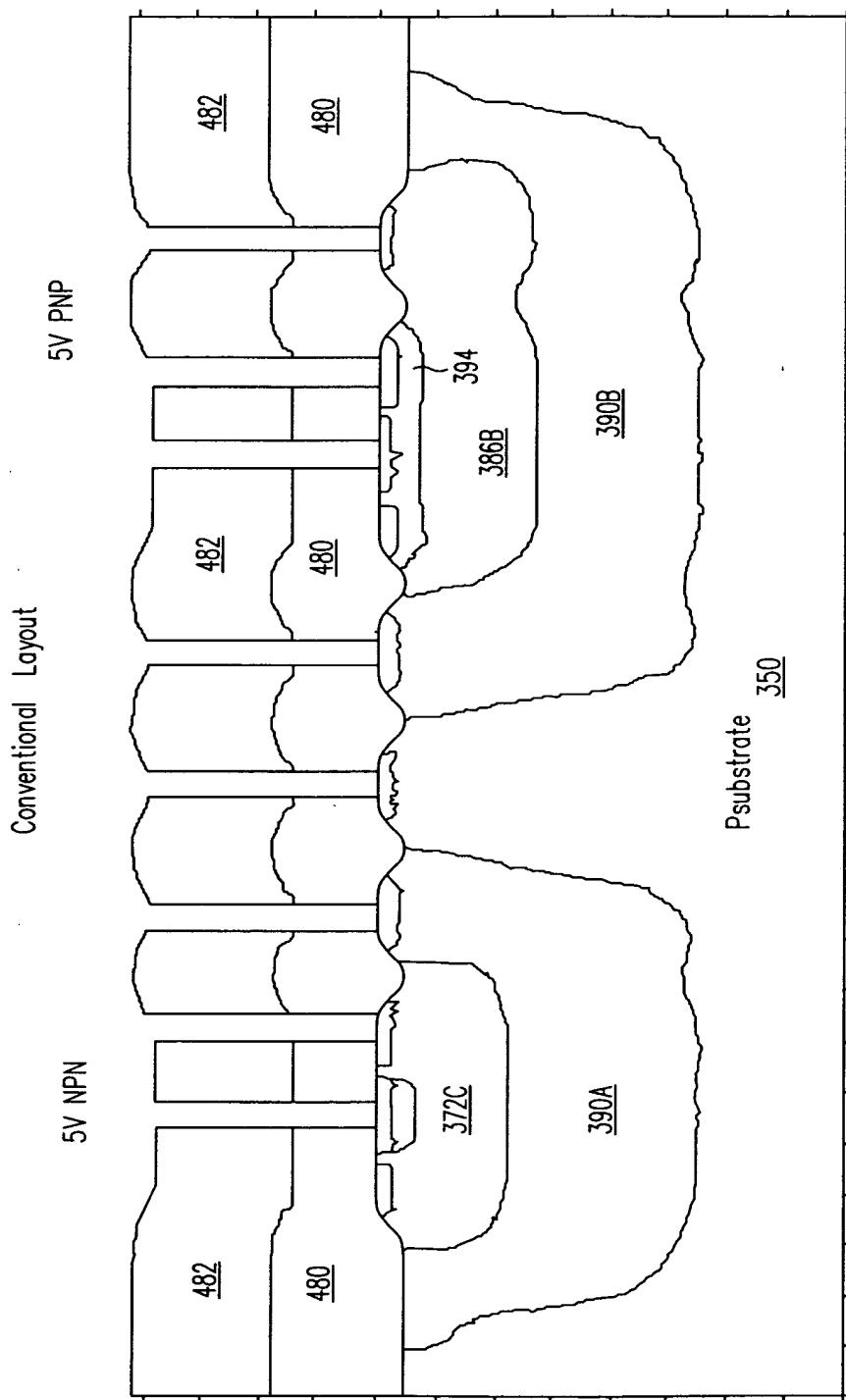
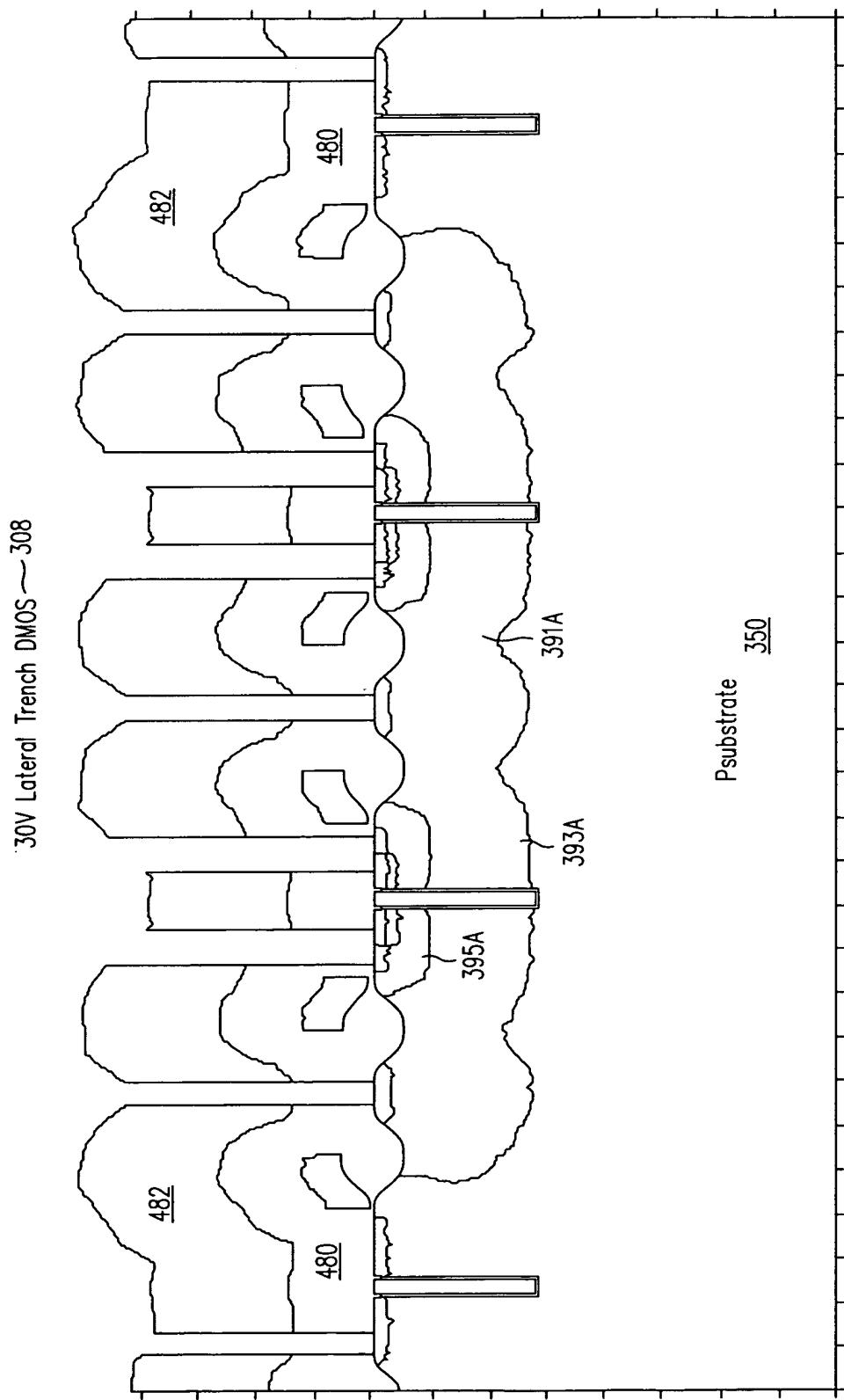


FIG. 64C

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Interlayer Dielectric Deposition and Etch

FIG. 64 D

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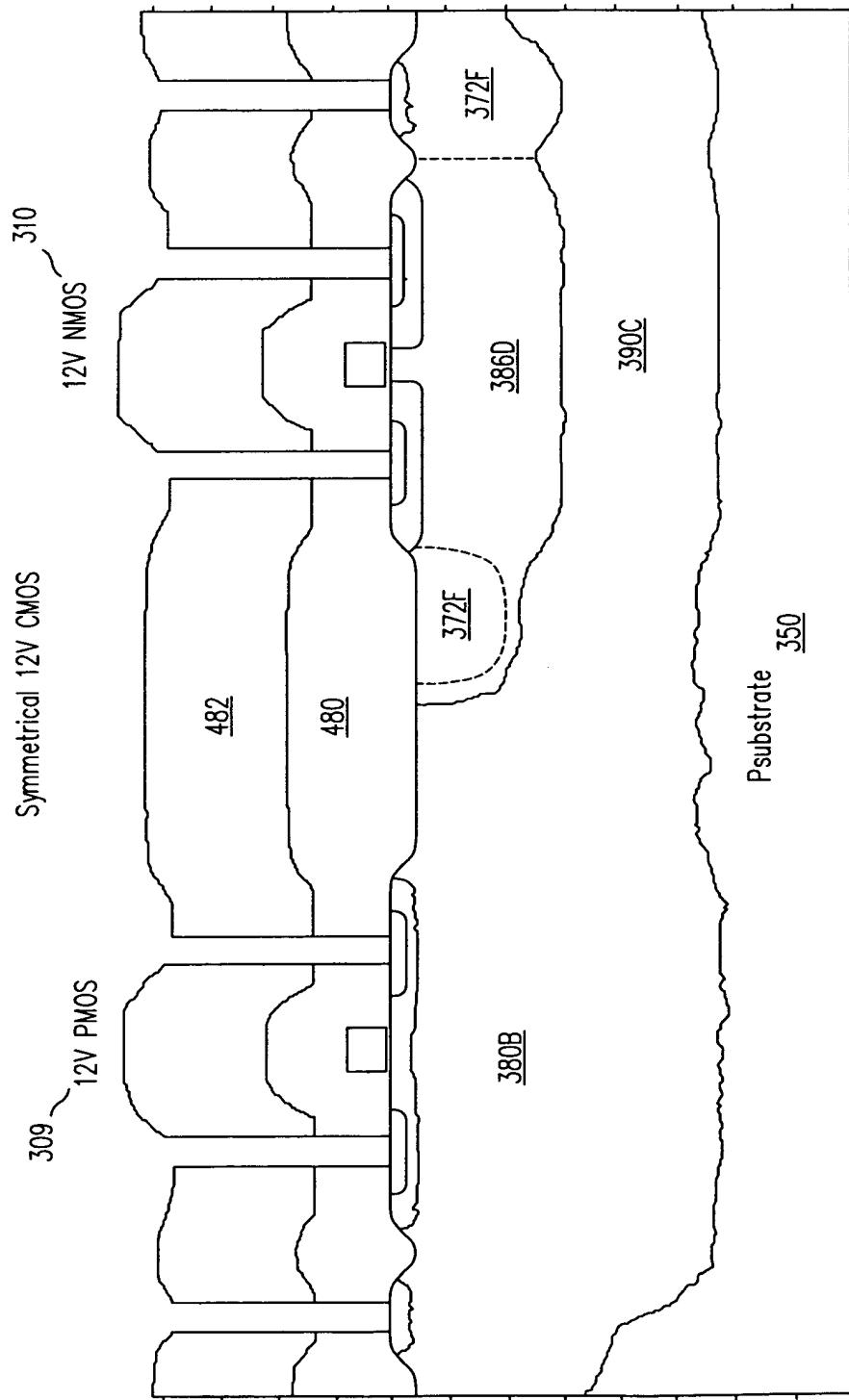
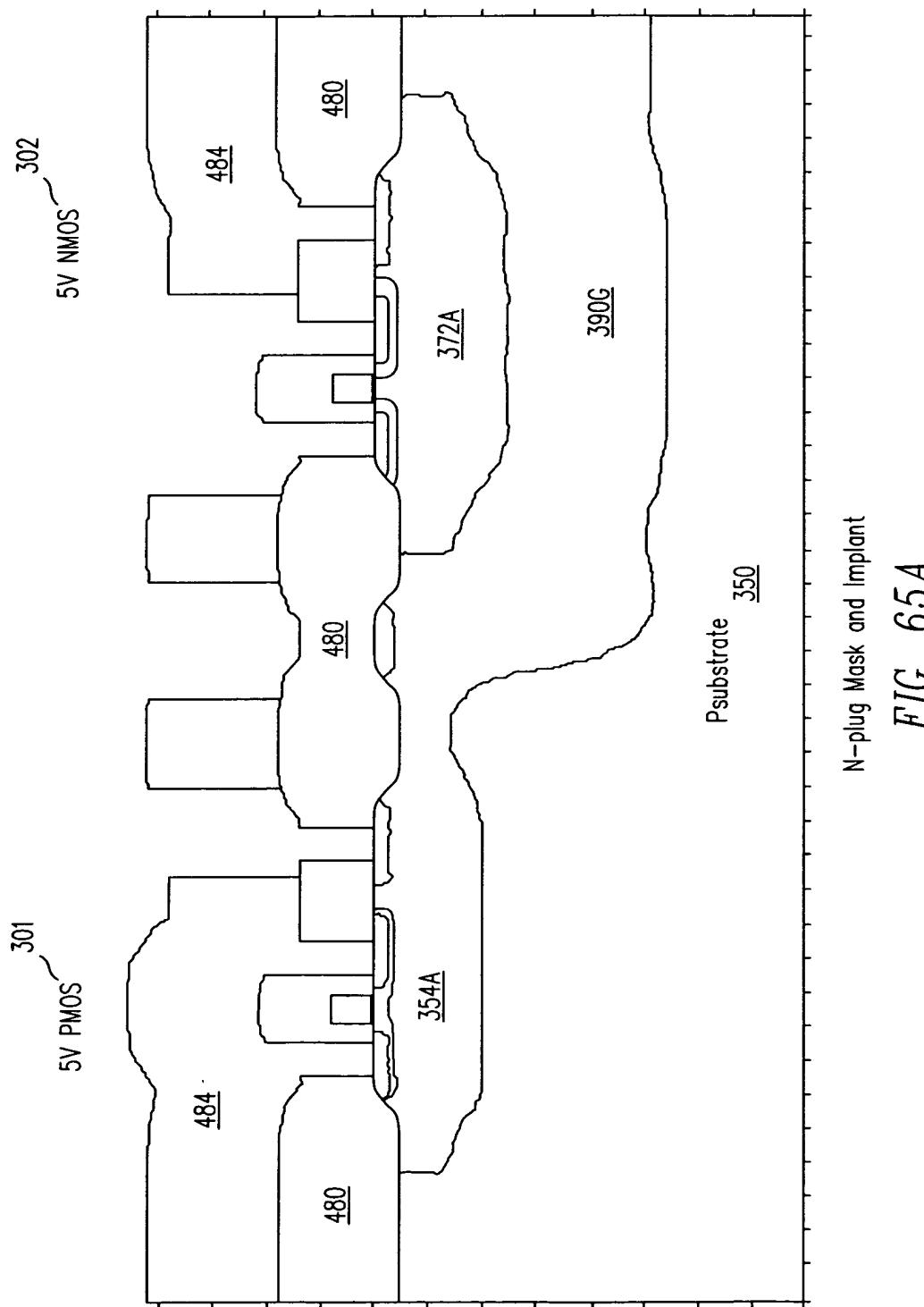


FIG. 64E

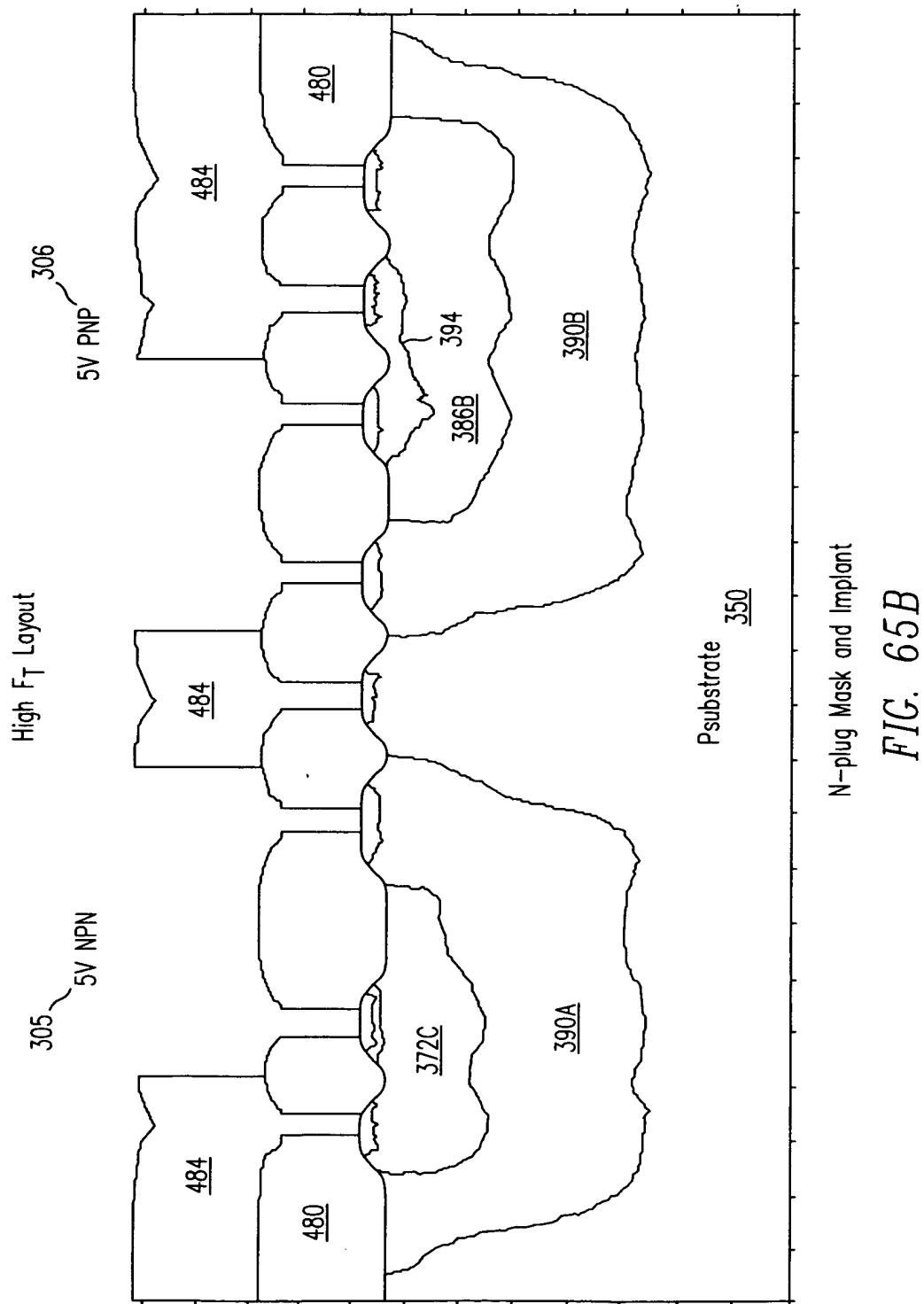
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N-plug Mask and implant

FIG. 65A

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N-plug Mask and Implant

FIG. 65B

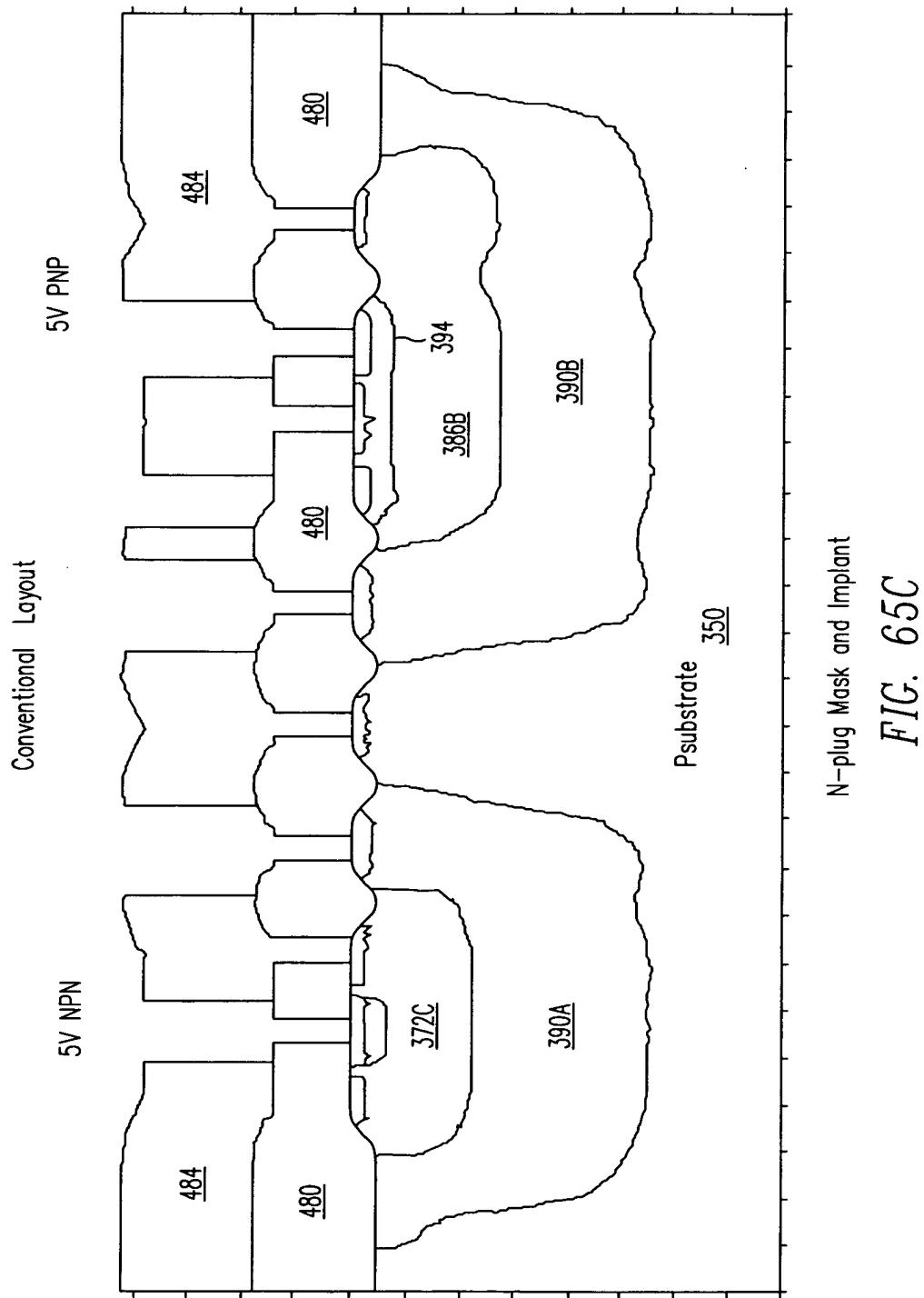
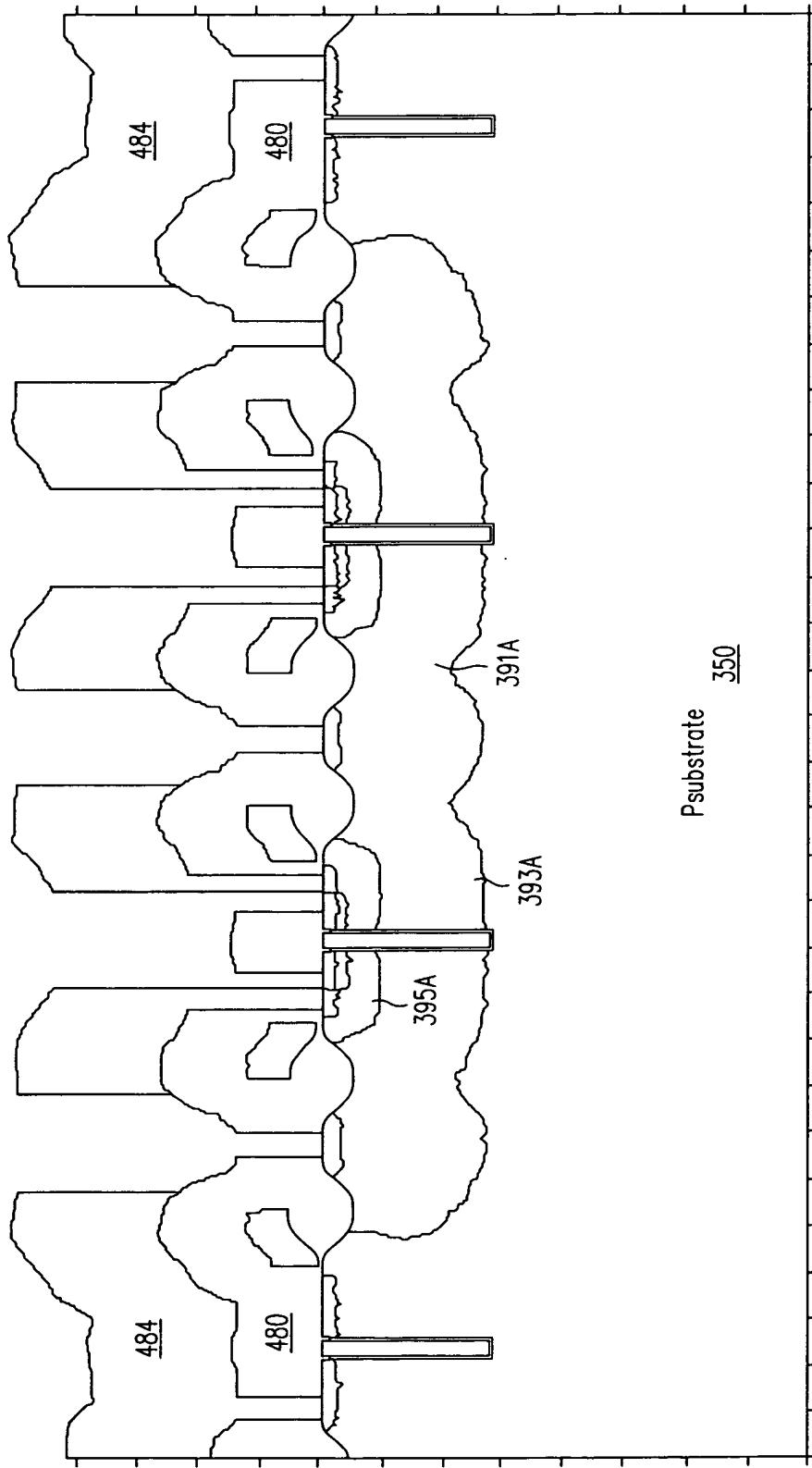


FIG. 65C

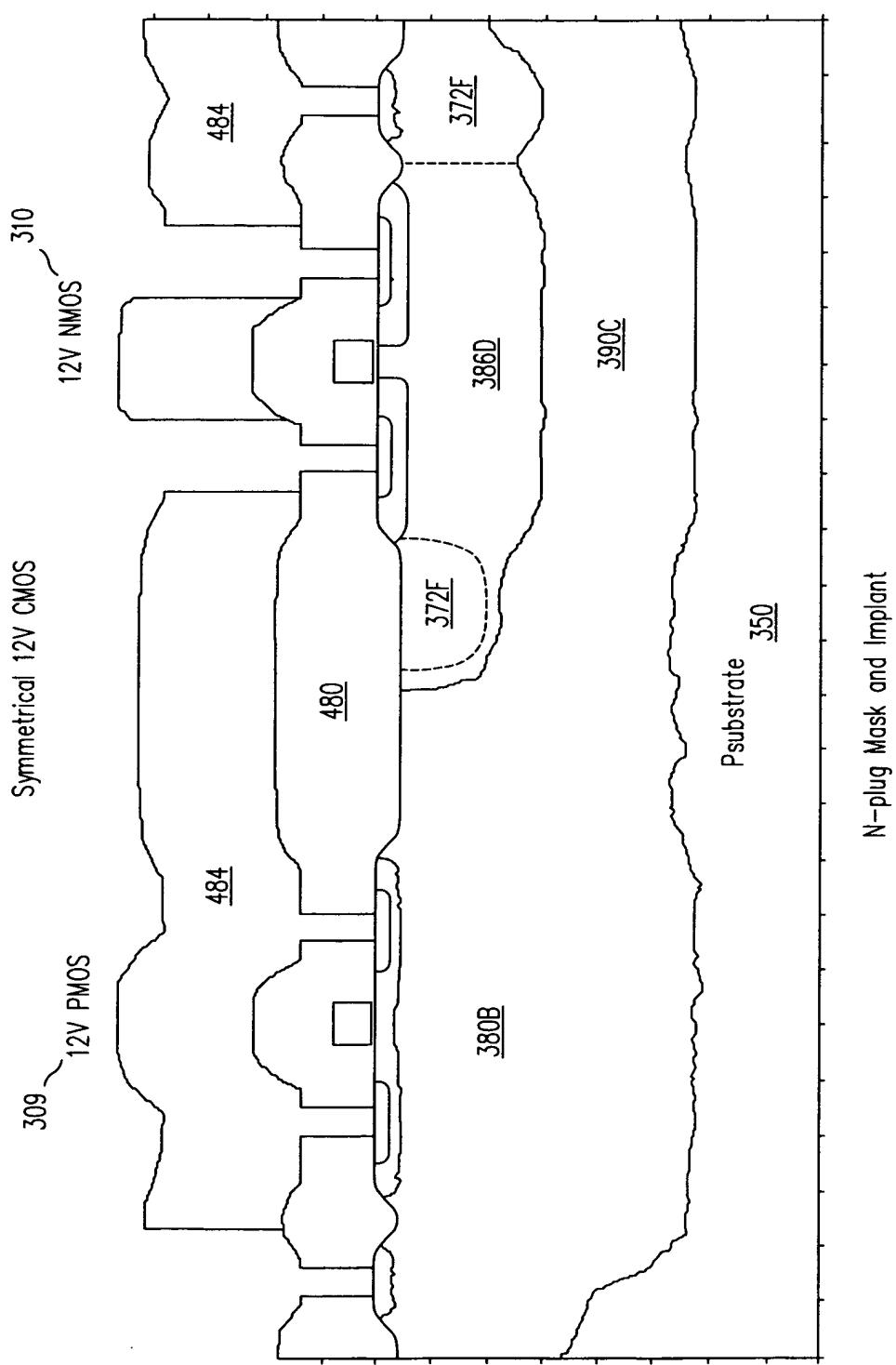
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N-plug Mask and Implant

FIG. 65D



N-plug Mask and Implant

FIG. 65E

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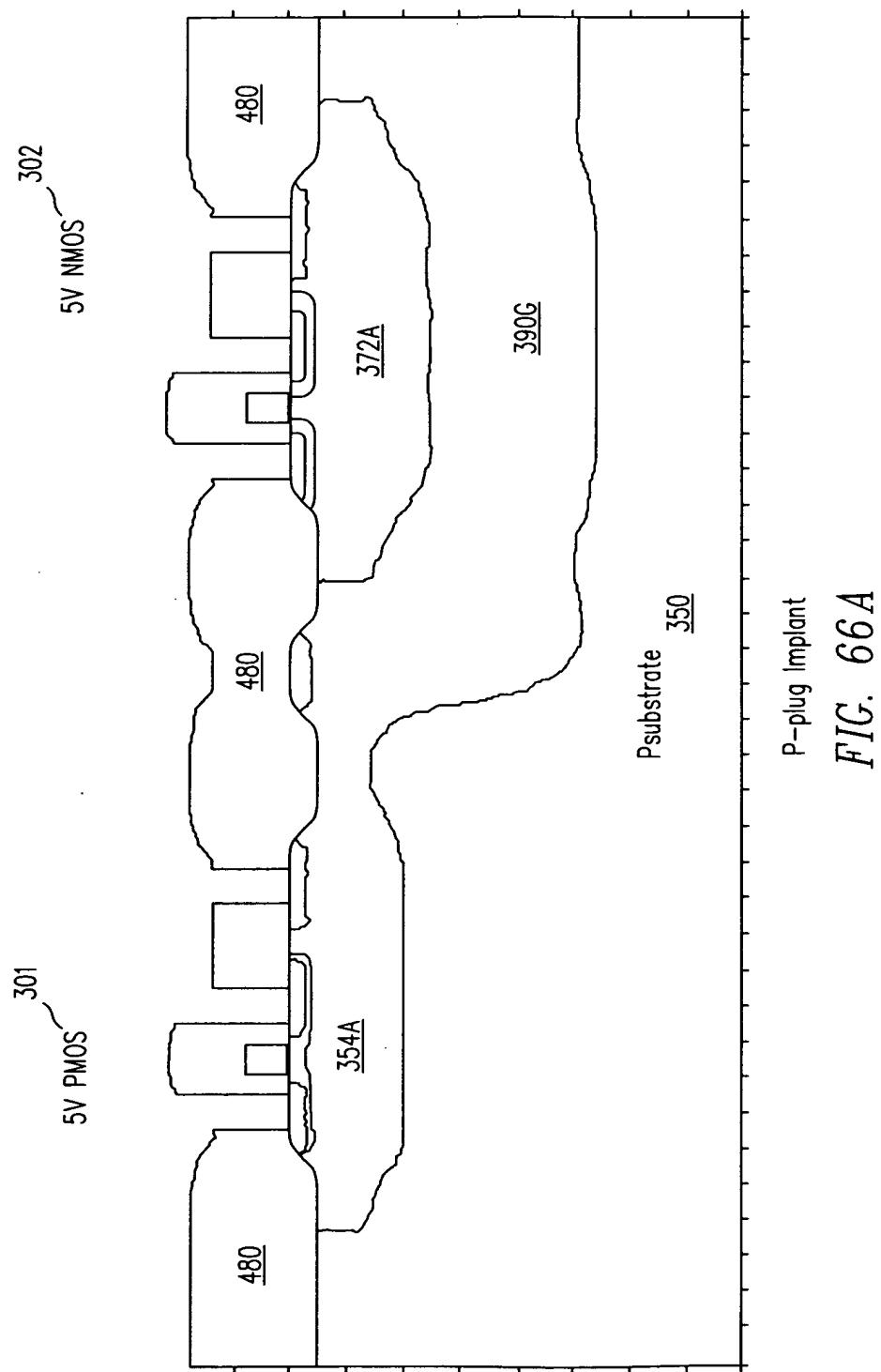


FIG. 66A

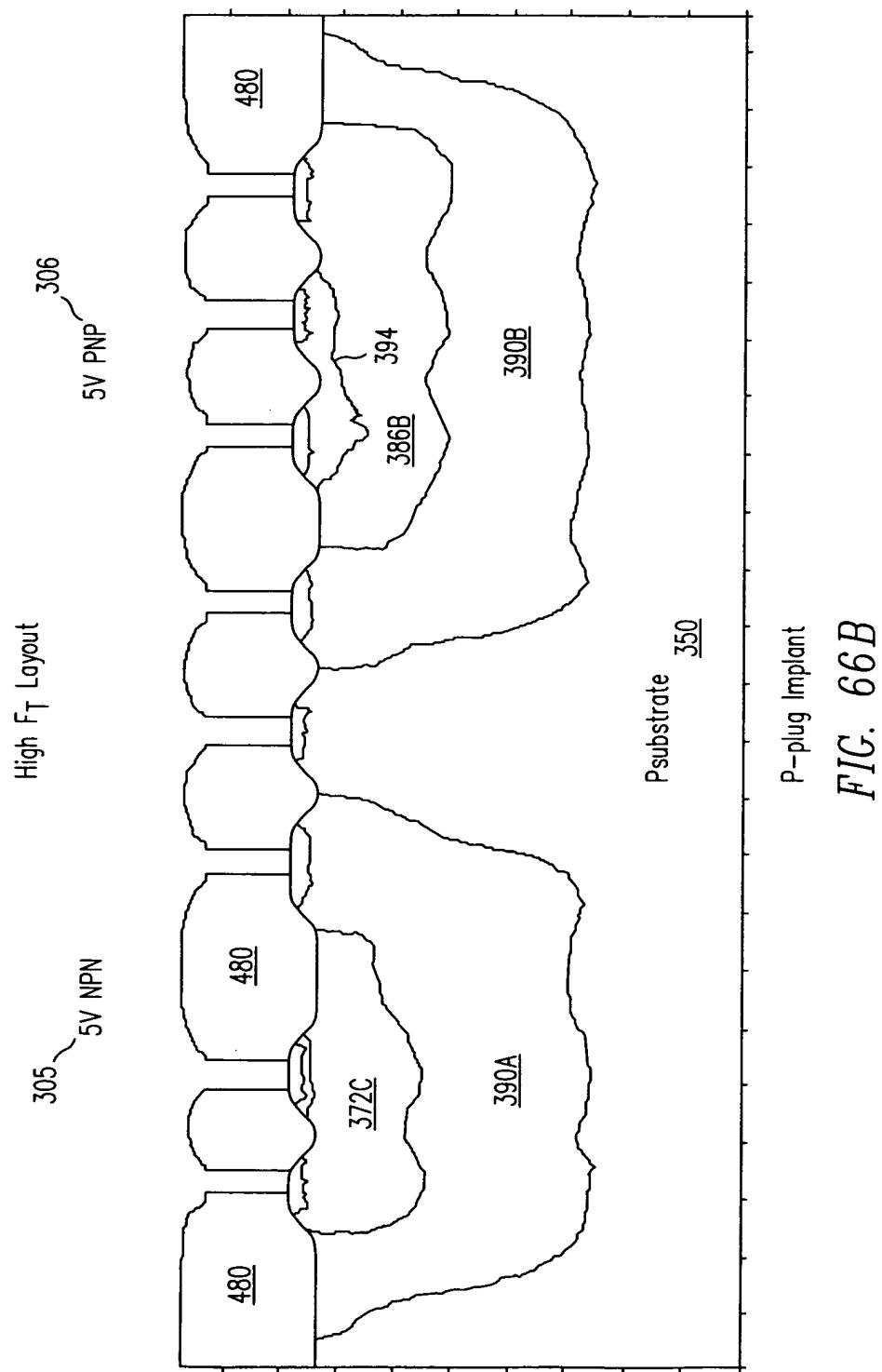
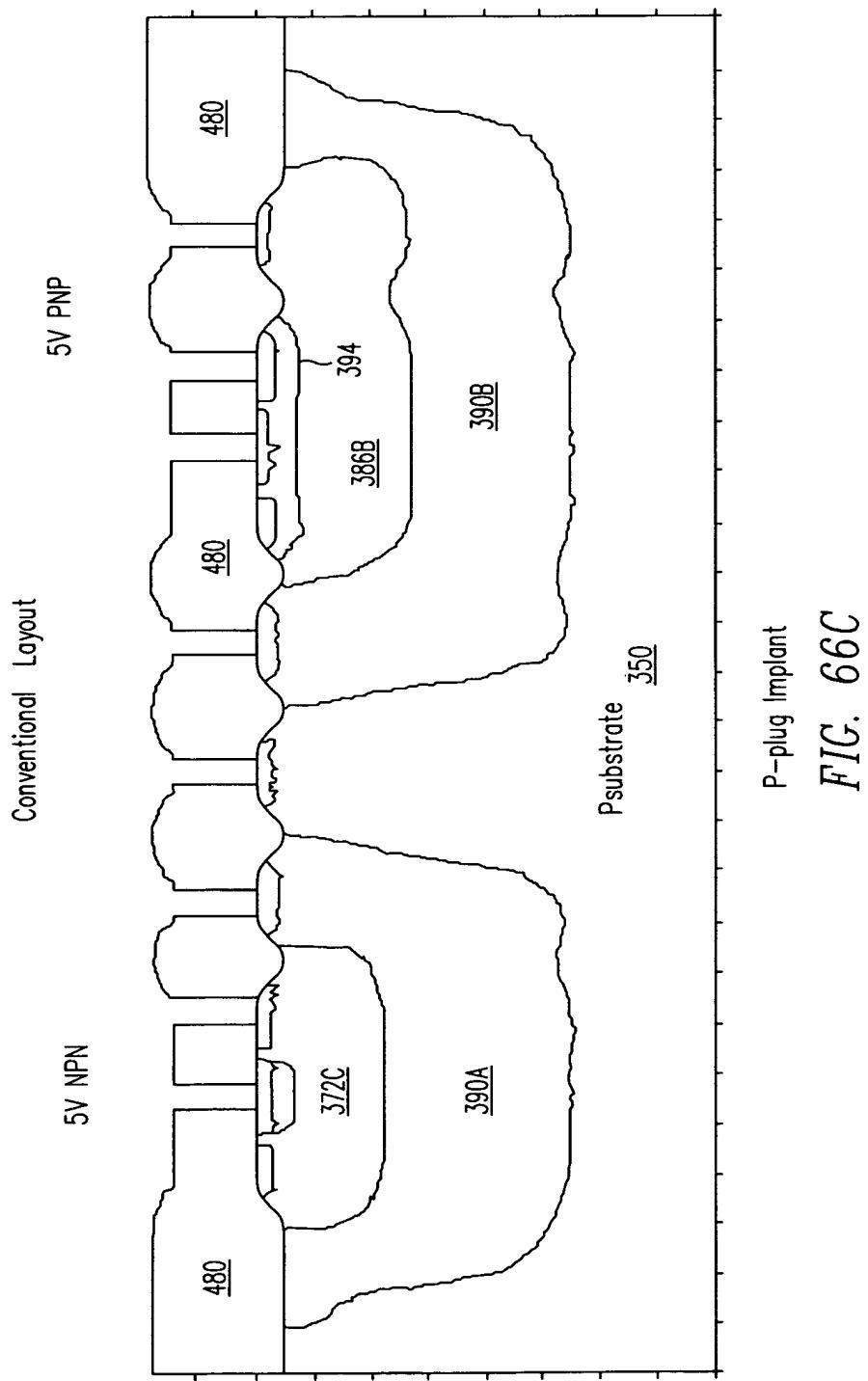
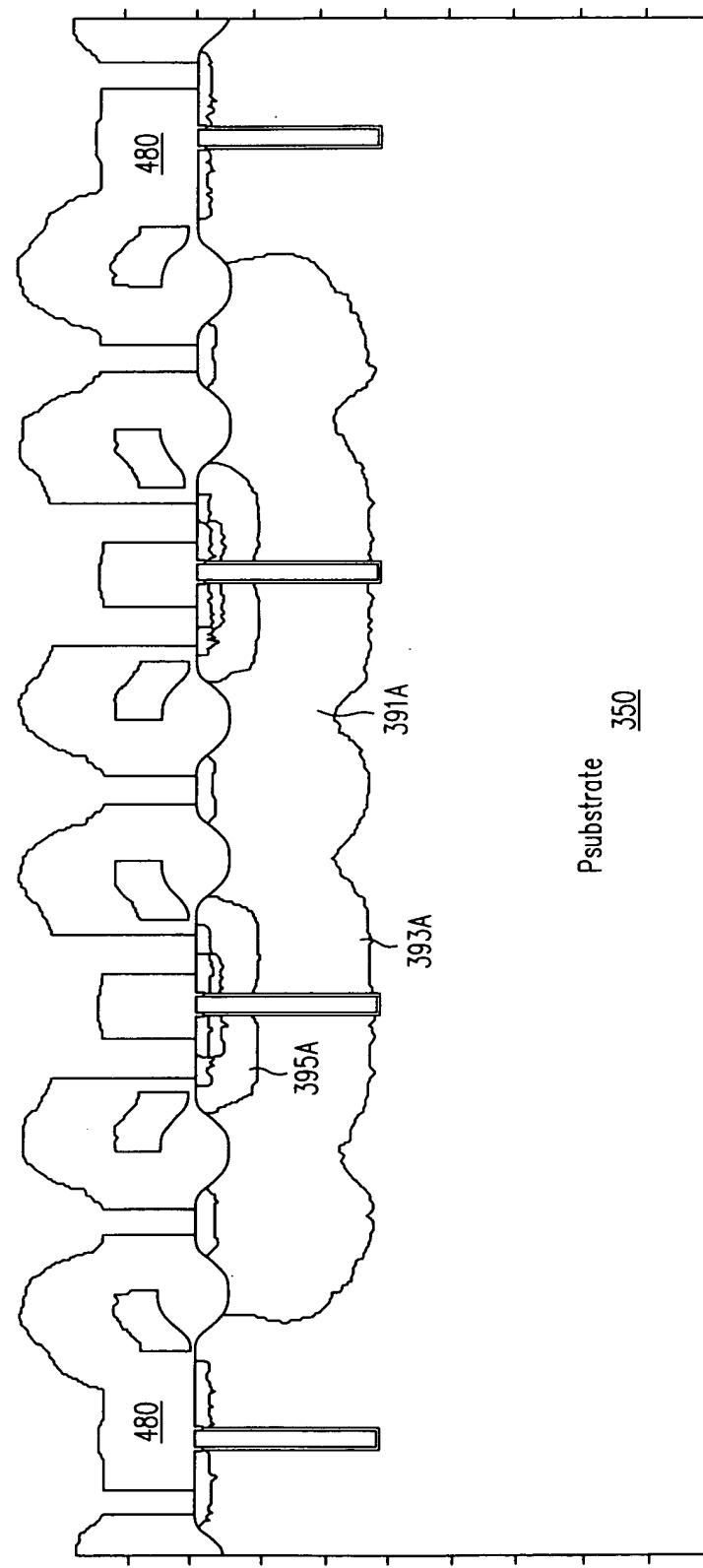


FIG. 66B



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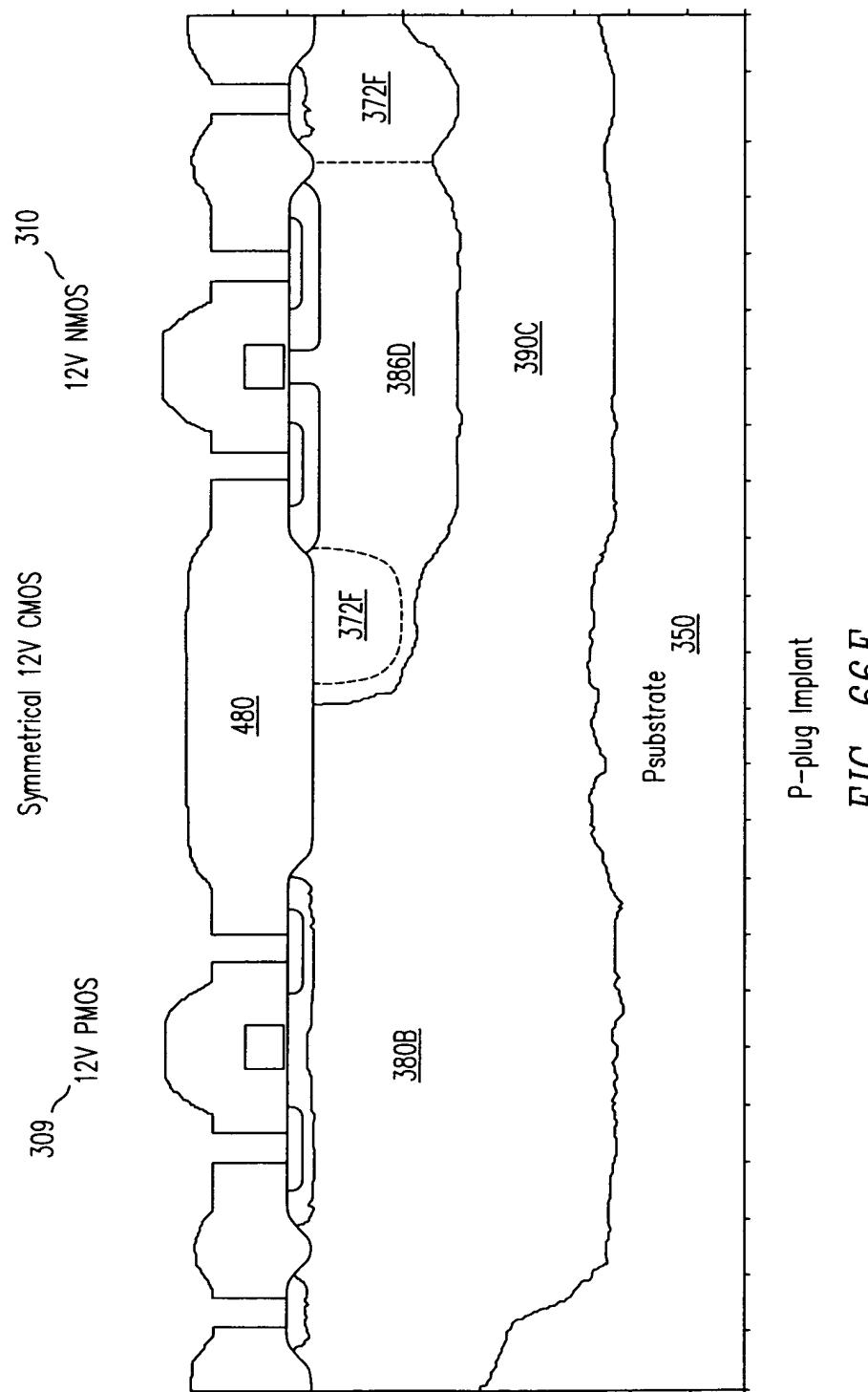
30V Lateral Trench DMOS — 308



p-plug implant

FIG. 66D

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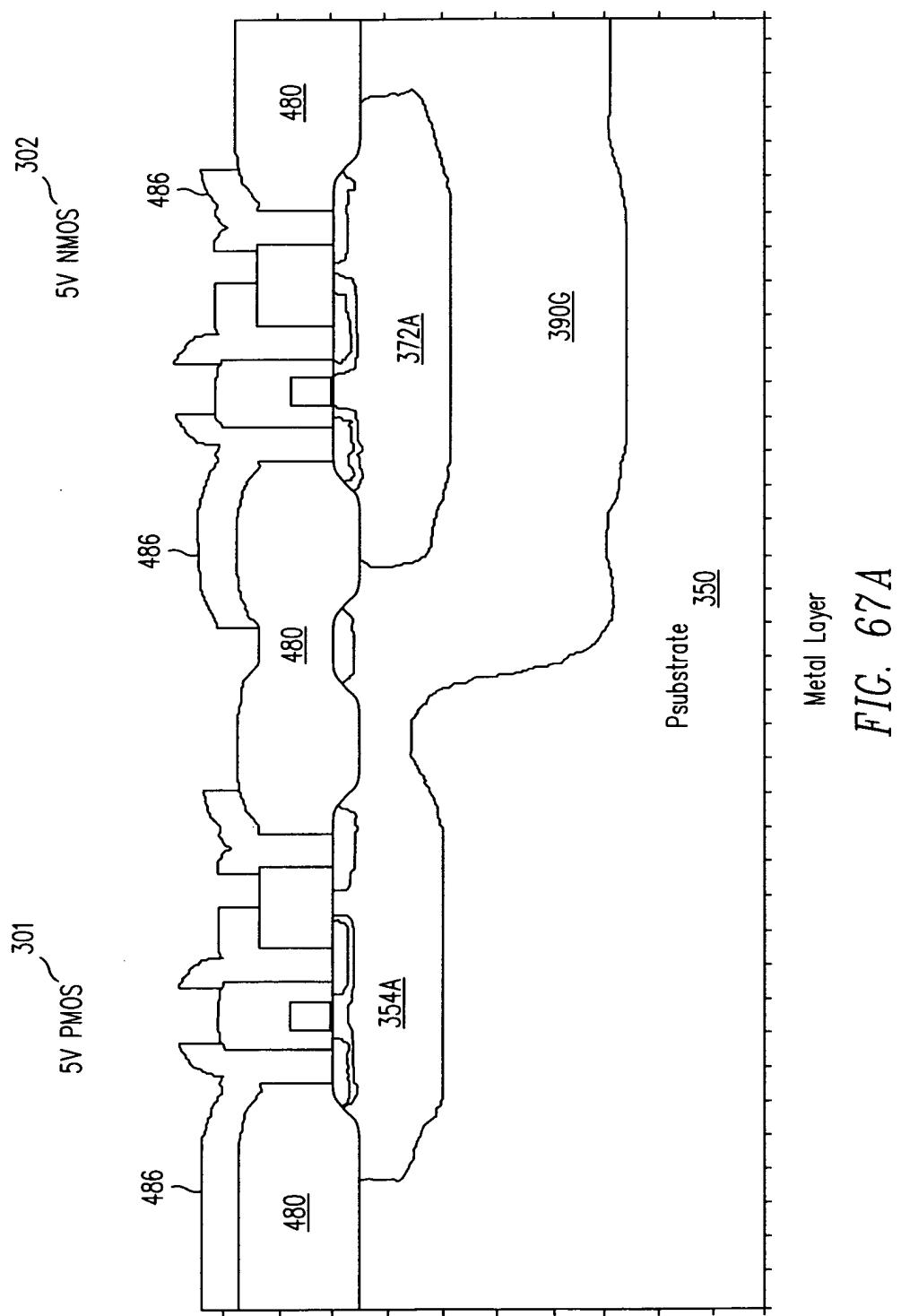
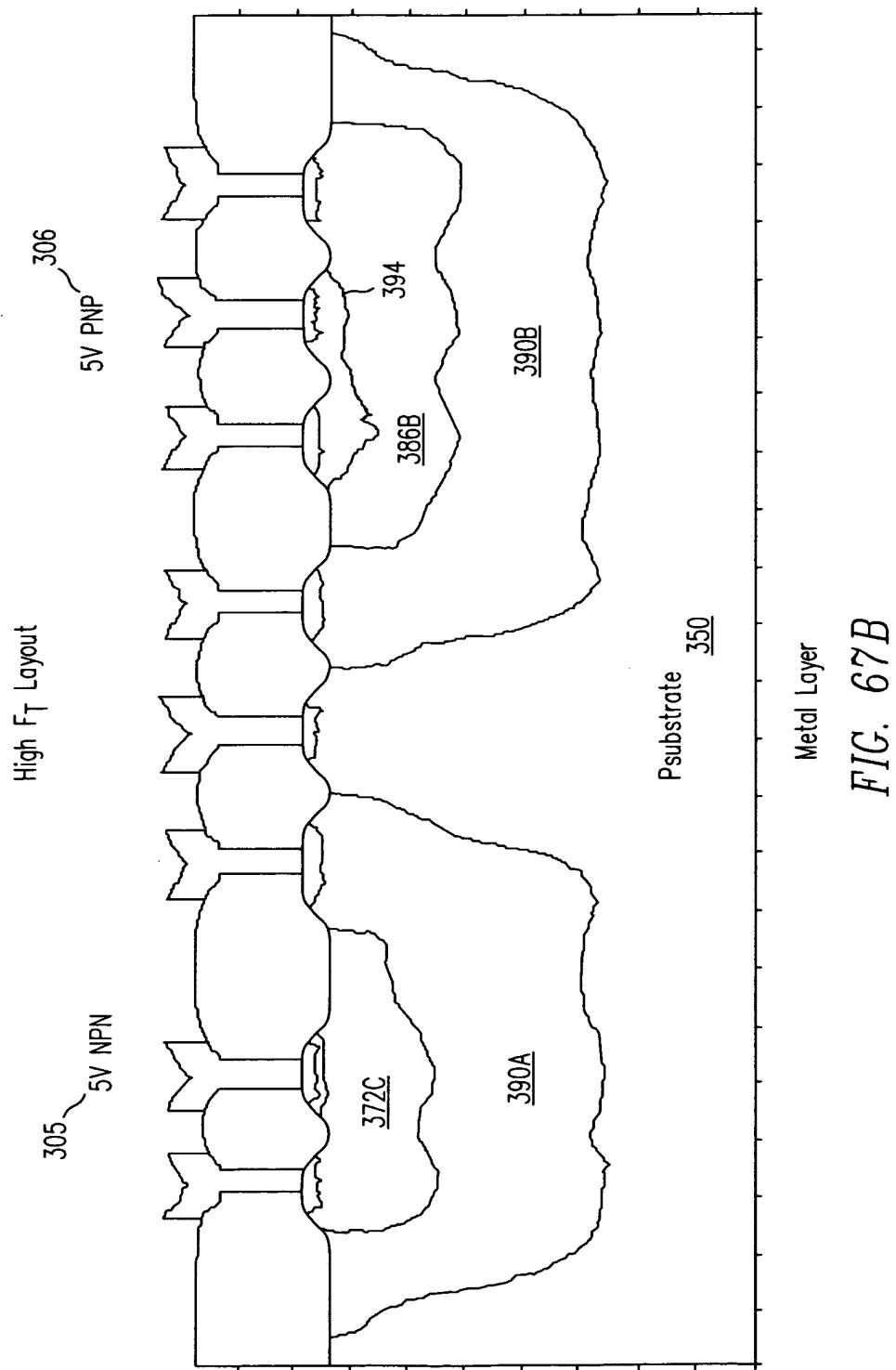


FIG. 67A

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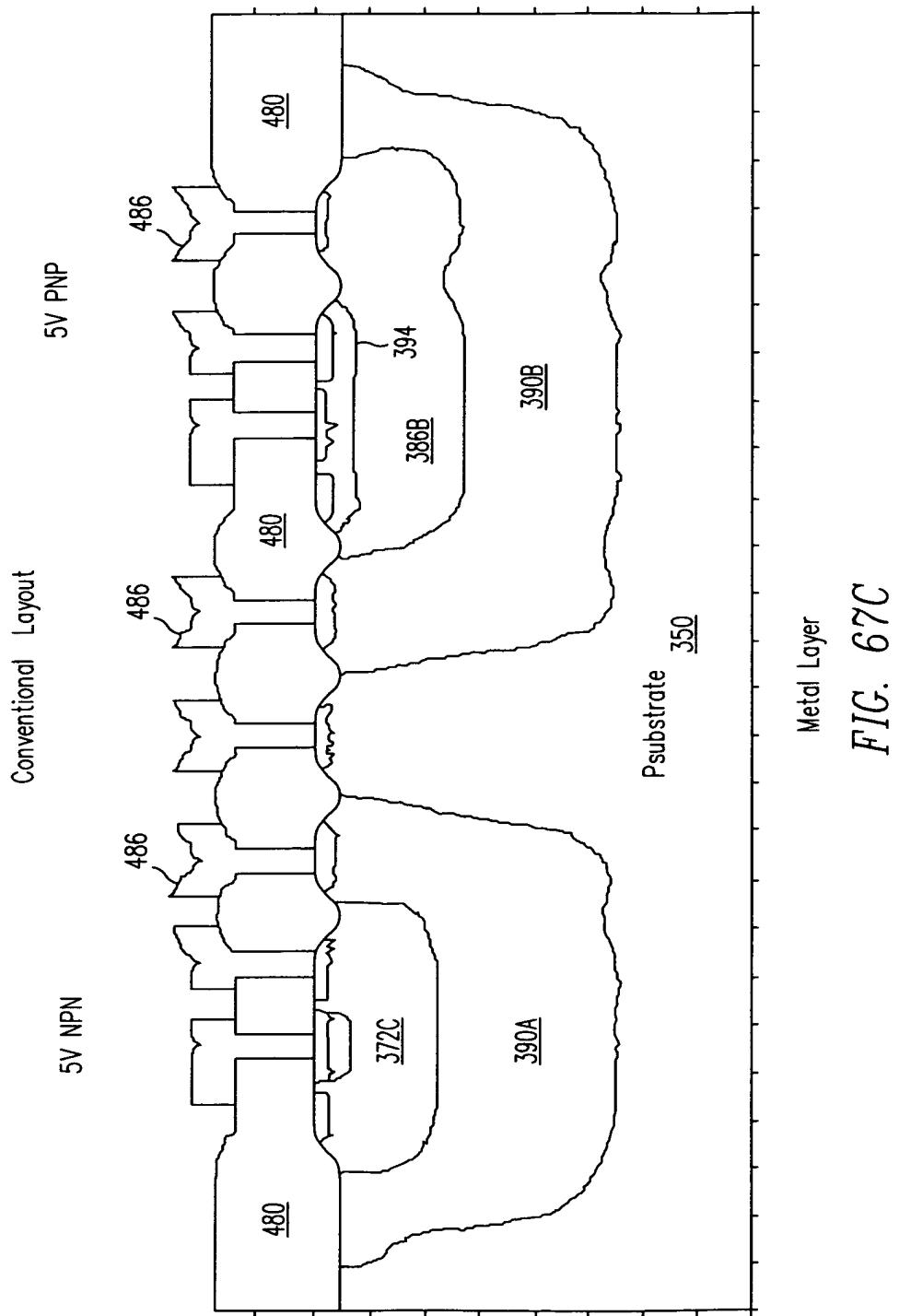


FIG. 67C

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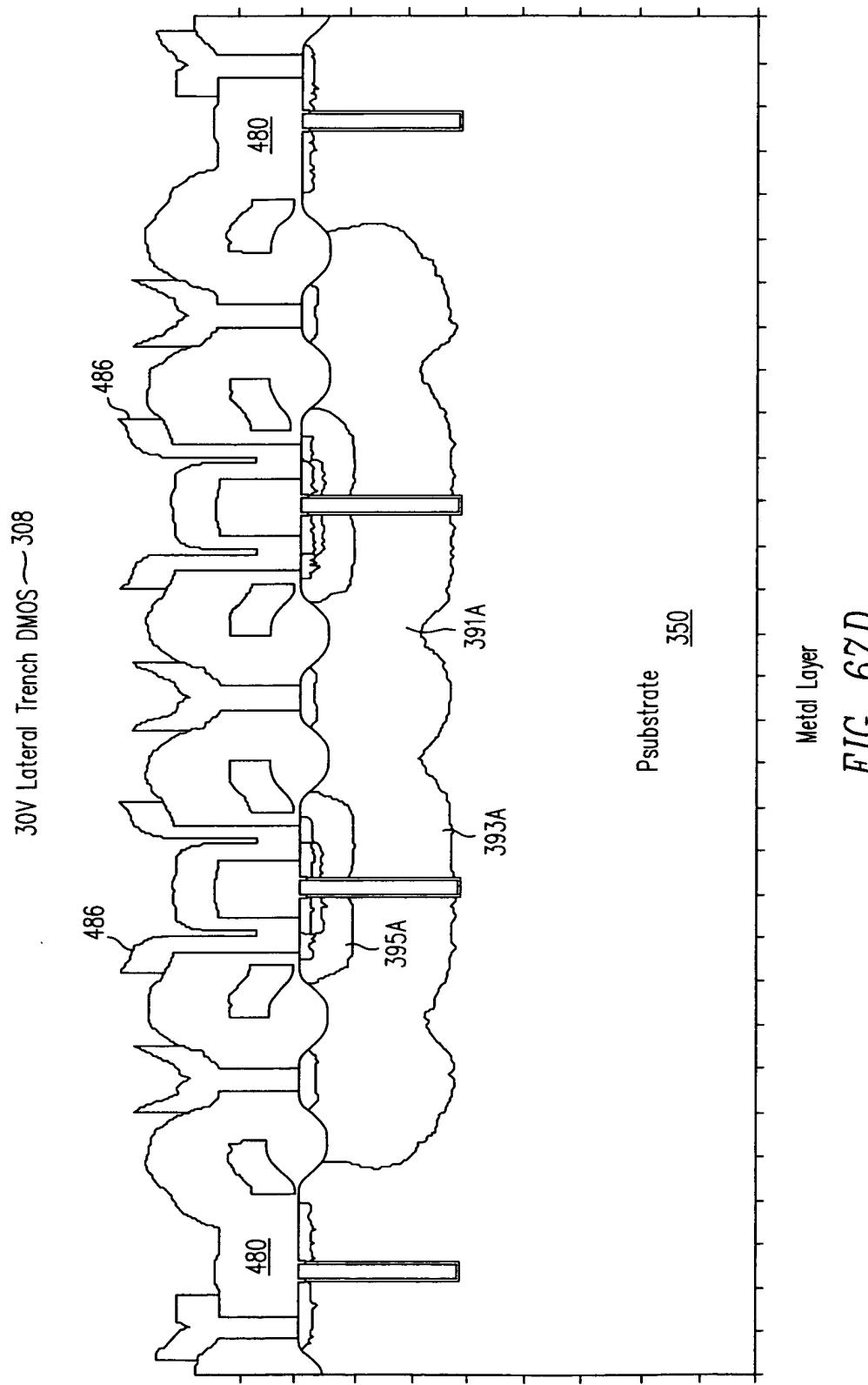


FIG. 67D

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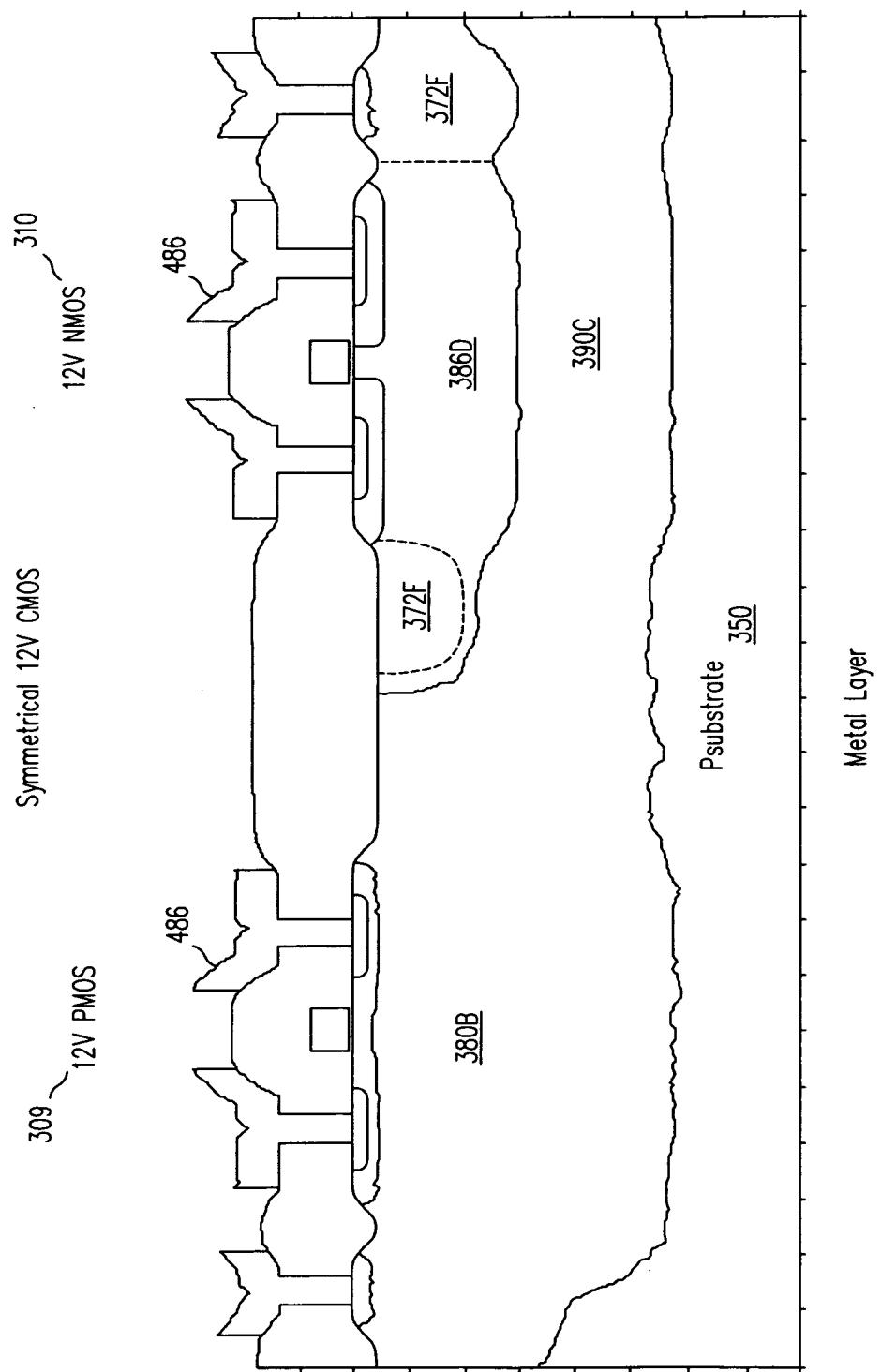


FIG. 67E

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